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Faculty of Science and Technology

A Class-E-Based AC-DC converter for PFC applications

Proposal of AC-DC PFC converter for a two-stage offline converter used in power electronics.

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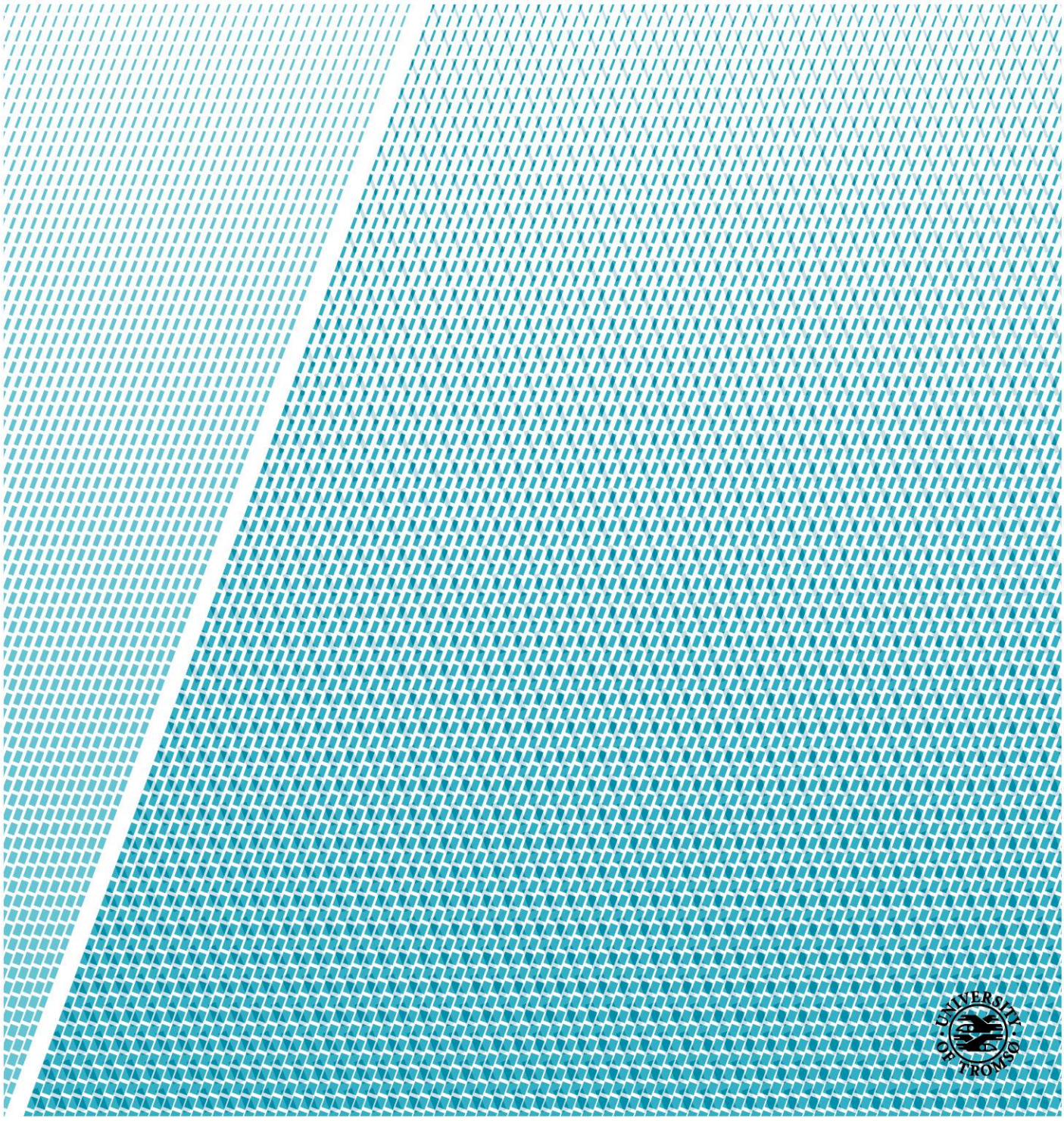

Foreword

This master thesis has been conducted though the fourth semester of electrical engineering at UiT campus Narvik. The objective for this thesis is to propose a converter for a two-stage offline power factor correction converter used in power electronics.

Power factor correction is used when using nonlinear loads to match the voltage and current to reduce the harmonic content injected into the grid. Working with this topic has increased my knowledge within power supply topologies and given me an insight into resonant converter.

Throughout this project, Bjarte Hoff and Hussein Mahdi Al-Sallami has been supervisors. I would give a sincere gratitude to Hussein for guidance and valuable knowledge needed to complete this assignment.

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Abstract

Connection of nonlinear utility load har increased through resent years and is expected to continue increasing. Nonlinear utility load injects harmonic content into the grid and reduces voltage quality for nearby consumers. To limit harmonic content from nonlinear load, the International Electrotechnical Commission requires power supplies to be designed according to IEC 61000-3-2. Fulfilling this standard for nonlinear load is done by power factor correction (PFC).

Conventionally, pulse width modulation (PWM) converter has been used for PFC converters as they provide high efficiency with a simple control technic. However, as PWM converters switch by hard-switching, that limits the switching frequency through switching loss and generates EMI, resonant converters has become more attractive. Resonant converters operate at soft-switching where the voltage across and/ or current through is zero in the switching moment. This reduces switching loss and EMI, and allow for high switching frequency. High switching frequency is desired as it enables high power density.

Through this thesis, two resonant converters using high switching frequency has been proposed. These converters are based on a Class-E converter as it has low noise and high efficiency when switching at high frequency. The thesis includes a mathematical model for both converts, simulation and experimental testing result. Result from testing differs from calculated and simulated values, and troubleshooting for one of the converters has been conducted. Through troubleshooting and a second test with changed parameters, the performance of the converter increased compared to the first test. Due to lack of time, the debugging process was not completed and will be a part of future work.

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1 Introduction

Increasing use of power electronics has strengthen the need for converters to supply a stable voltage with low ripple and harmonic content. It is expected that more than 60% of utility load will be nonlinear within 2025 [1]. The growing use of nonlinear loads increases the need for offline AC/DC converters with power factor correction (PFC) capabilities, as nonlinear loads produce harmonic content that is injected into the grid. Harmonic content reduces the voltage quality and have adverse effects on electronic equipment connected nearby [1]. To limit harmonic content, the International Electrotechnical Commission regulates the amount of harmonic through IEC 61000-3-2.

An offline AC/DC converter consists of two converters separated with a DC link capacitor, as shown in Figure 1. The first converter is an AD/DC converter that works as a rectifier with PFC capabilities and limits the amount of harmonic content fed back into the grid. The second converter is a DC/DC converter that regulates the voltage by stepping it up or down depending on the desired voltage.

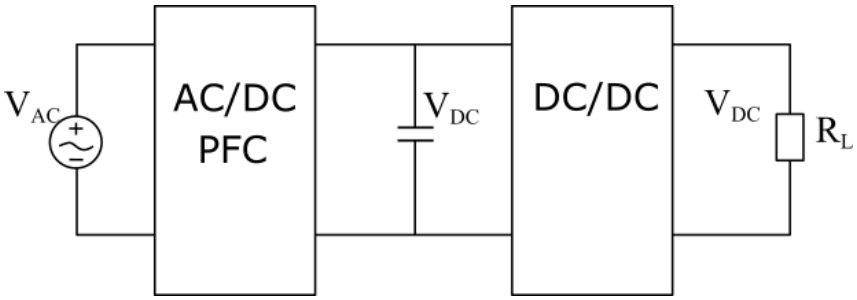

Figure 1. Offline convert structure

Project objective

This project is to propose an AC/DC PFC converter for a two-stage converter used in power electronics, such as lighting application. The proposed converter should for work with 1 MHz switching frequency to reduce the size of the converter, and hence, increase the power density.

The project suggests two converters based on a Class-E converter with switching frequency of 1MHz. The first suggested converter is based on the design of a Class-E based converter used for PFC in [2]. The second suggested converter is based on Class-E^2 converter from [3] where it is proposed as a high-efficient DC-DC converter.

Limitations

Throughout experimental testing of the proposed converters, it has been a limitation to not measure the current. Measure the current would have increased the understanding of the circuit

behaviour and given a better comparison between simulated, calculated, and experimental results. Thus, the plan was to build a current measure PCB to connect in series with the resonant circuit. Due to late shipping, these components did not arrive until after project deadline. Therefore, the experimental result does not contain high-frequency current measurements and plots.

1.1 Power factor correction

Power factor correction (PFC) converters intends to emulate a resistor from the source and minimize the reactive power drawn from the grid. PFC converters can be used in application, such as frequency converters or renewable energy sources. The most common way of arranging this is placing the PFC application between the rectifier bridge and the storage capacitor, as shown figure 2 [4].

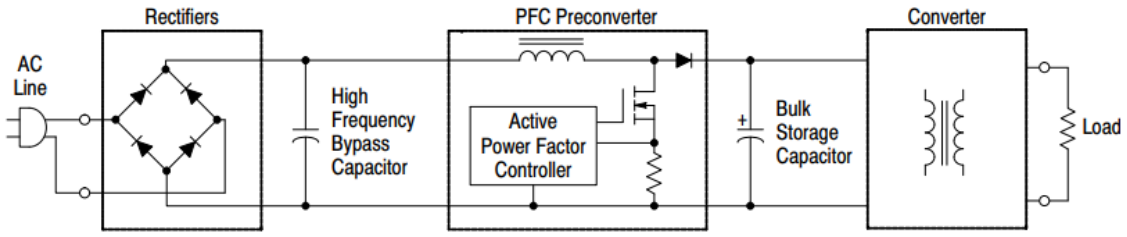

Figure 2. Offline AC-DC converter with power factor correction [4].

Power factor is defined as the ratio between the real and apparent power, as shown [4]:

$$PF = \frac{Real\ power}{Apparent\ power} \tag{1,1}$$

Real power is the average over a cycle of the instantaneous product of current and voltage while the apparent power is RMS values of the current and voltage over a cycle [4]. In circuitry with only passive components, the power factor is given by the displacement factor between current and voltage. If the circuitry consists of active components that generate a distorted voltage, as in figure 2, the power factor consists of both a displace factor and a distortion factor. Real power entails the fundamental component of the current, 50Hz, while the higher order of the fundamental component is harmonic distortion and contributes to apparent power. The harmonic content is measured by an index called total harmonic distortion, THD, and is given by the relationship [4]:

$$THD = \sqrt{\sum_{p=2}^{\infty} \frac{I_p^2}{I_1^2}} \quad (1,2)$$

Where p- is the number of the harmonic order and I_1 is the first harmonic order current, also called the fundamental component. The THD is regulated by IEC 61000-3-2 where each of the harmonic order has maximum limits. This limitation controls the pollution of the input current and has the intention of minimizing the input current and interference [4]. Figure 3 shows two voltage and current plots with a high and low content of THD. Figure 3a shows high harmonic content due to distortion of the sinusoidal waveform of the grid current, while figure 3b shows a sinusoidal gird current following a low content of harmonics [4].

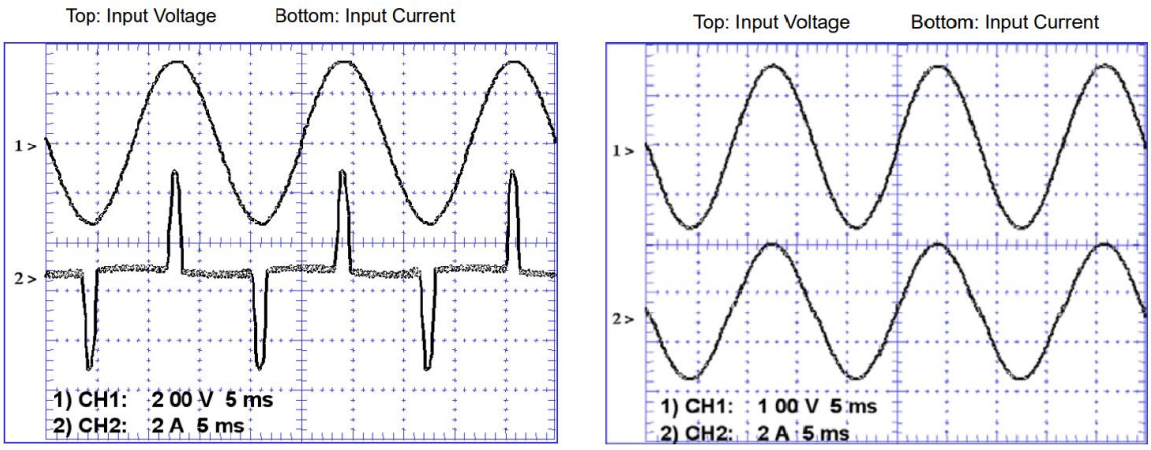

Figure 3a shows low power factor and a high amount of harmonic distortion. Figure 3b shows low harmonic and a power factor close to one [4].

1.2 Harmonic Limits

IEC 61000-3-2 limits the harmonic current injected into the power grid [5]. The standard accounts for equipment with a rated current up to and including 16 A per phase and rated voltage of 220/380 V, 230/400 V and 240/415 V [5].

Classification of equipment

Equipment that is regulated under this standard are divided into classifications from Class A to Class D [5]. These classes are described as following:

- Class A includes equipment not specified under the other classes, from Class B to Class D, with examples such as:

    - Balanced three-phase equipment, household applications (not included in Class B to Class D), vacuum cleaners, high pressure cleaners, tools (Not portable), independent phase control dimmers and audio equipment.
- Class B includes portable tools and arc welding machines (not professional).
- Class C includes lighting equipment.
- Class D includes following equipment (specified power less than or equal to 600W):
    - Personal computers and personal computer monitors, television receivers, refrigerators and freezers having one or more variable speed drives to control compressor motor.

Limits of Class C

As the proposed circuits is design for lighting equipment, the harmonic is limitation by the Class C limitations, and hence, taken into consideration during testing and comparison. Maximum limits for equipment in Class C with a higher rated input power than 25 W is found in table 1 as a percentage of the fundamental frequency [5]. The limit assumes a power factor equal or higher than 0.9. Harmonic number which is not listed in this table does not have a limit for this class under these conditions.

Table 1. Harmonic order and maximum limits [5].

Harmonic order, *p*	**Maximum limits,** %
2	2
3	27
5	10
7	7
9	5
$11 \leq p \leq 39$	3

1.3 Power supplies

Power supplies are needed to provide a ripple-free voltage and often called voltage regulators. There are different power supply technologies available with different advantages and disadvantages. Dividing power supplies into two types of voltage regulators gives linear regulators and switching regulators. Linear regulators operate the transistor within its linear region, resulting in a high voltage drop across the transistor. This gives a large power dissipation and low efficiency which makes the converter larger than switching regulators. Switching regulators, also called switch mode converters or switch mode power supplies (SMPS), utilise

transistors as switches. Switching regulators have high efficiency, high energy density, and are small in size. In addition, they have the ability of connecting several outputs. Switching regulators can be divided into pulse-width modulation (PWM) converters and resonant converters, as shown on figure 4 [6].

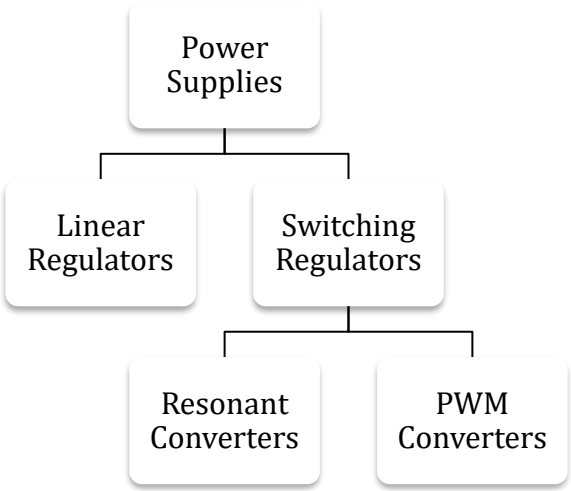

Figure 4. Power supplies divided into Linear Regulators and Switching Regulators.

Linear regulator has more recently been adopted into PFC circuits together. In paper [7], a linear PFC regulator has been proposed for LED lightning applications. Paper [8] uses a buck PFC converter with a linear regulator to drive and control the current of power LEDs.

2 Topology overview

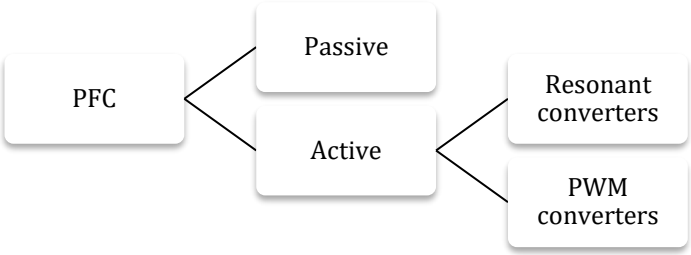

Figure 5. PFC topologies divided into active and passive circuits.

Power factor correction can be achieved through ether active or passive circuits. Passive PFC converters uses inductances and capacitors to filter the current drawn from the grid. Paper [9]–[11] shows how inductances and capacitors can be used to filter the input current. The drawbacks of using passive filtering for PFC is the need for large inductors and capacitors which results in a large converter. An active PFC converter uses active components to shape the input current to match the input voltage[4]. Active PFC consists of active components such as transistors. or integrated circuits. As illustrated in figure 5, active PFC converters are further divided into Resonant and PWM converters.

PWM converters has a higher switching loss than resonant converters due to hard switching, Hard switching and trapezoidal voltage causes harmonics and EMI [6]. Resonance converter operates at soft-switching in which the voltage across and/or current through the transistor is zero, or close to zero. Operating at soft-switching reduce EMI and switching loss [6]. The soft-switching capability makes the increase of switching frequency possible, and hence increase the energy density and reduce the component size [6].

Switching losses are due to a transistor output parasitic capacitance, a diode parasitic capacitance, diode reverse recovery, and inductance leakage. Soft switching can be either zero voltage switching (ZVS) or zero current switching (ZCS). When ZVS, the voltage across the transistor is zero when switching on and off the transistor. This ensures there is no energy stored in the parasitic capacitance of the transistor. When ZCS, the transistor turns off at zero current [6].

Parasitic capacitance is an effect occurring as two conducting material with isolation between have applied voltage across. This effect has a non-linear characteristic that changes with the applied frequency, voltage, and structure of the component. In a MOSFET, there are three terminals with parasitic capacitance between, as shown on figure 6 [12].

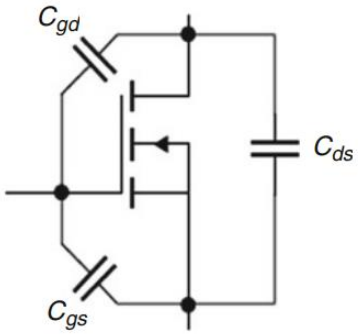

Figure 6. MOSFET with parasitic capacitanse

The transistor has a parasitic output capacitance which holds energy when voltage across. This energy results in power loss during switching in hard-switching converters and soft-switching converters if not ZVS is achieved. The stored energy in the parasitic capacitance has relationship:

$$W = \frac{1}{2} * C * V^2 \tag{2,1}$$

Where W is stored energy, C is parasitic capacitance and V is the drain-to-source voltage in switching moment. This results in power loss in the transistor at switching moment through following relationship:

$$P_{sw} = \frac{1}{2} * f * C * V^2 \tag{2,2}$$

Where P_{SW} is power loss and f is switching frequency. In (2,2), the power losses are proportional to the switching-frequency. Thus, increasing the switching-frequency results in increasing switching-losses.

2.1 PWM

PWM converters can be divided into many topology classifications. This chapter gives a brief introduction of some of the basic topologies. Figure 7 shows the classification of PWM converters. The converter are divided into bridge and bridgeless depending on the use of a diode

bridge for rectifying the alternating current. Using a diode bridge gives unidirectional power flow, while bridgeless topology gives possibility of a bidirectional power flow. Paper [13] gives a review of bidirectional and unidirectional power flow topologies.

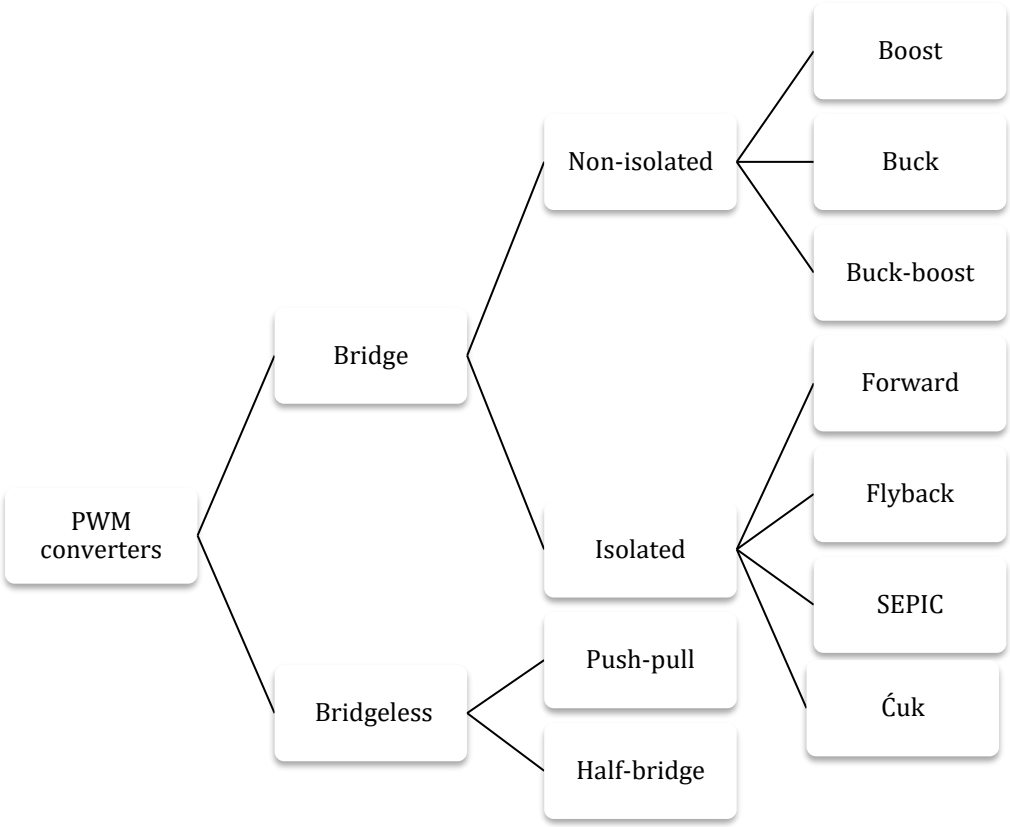

Figure 7. PWM converter divided into bridge and bridgeless converters.

Non-isolated

The bridge PWM converter can be further classified into isolated and non-isolated. Non-isolated is divided into boost, buck, and buck-boost, depending on increasing or decreasing the output voltage. Buck and boost converter are the two basic converters [14]. Boost converter increases the output voltage, buck decreases the output voltages and buck-boost can both increase and decrease the output voltage. However, buck-boost converter inverse polarity of the output voltage [6]. These topologies are shown in figure 8 [6]. Boost converters are widely used in PFC due to the simplicity, grounded transistor, small input inductor and high efficiency. Its disadvantages are switching loss and voltage limitation [15]. Buck converters are not ideal for PFC because its line current has crossover distortion, meaning that it has zero current when input voltage is smaller than output voltage [15].

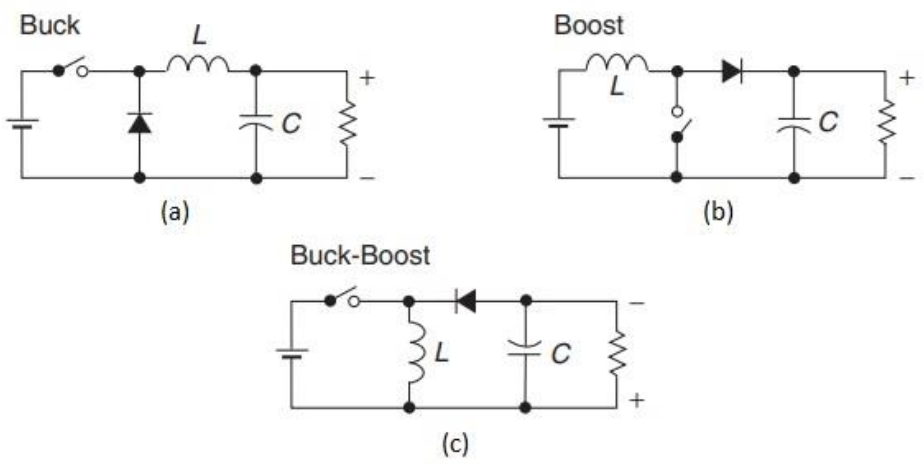

Figure 9. Buck, boost and Buck-boost converter topologies [6].

Isolated

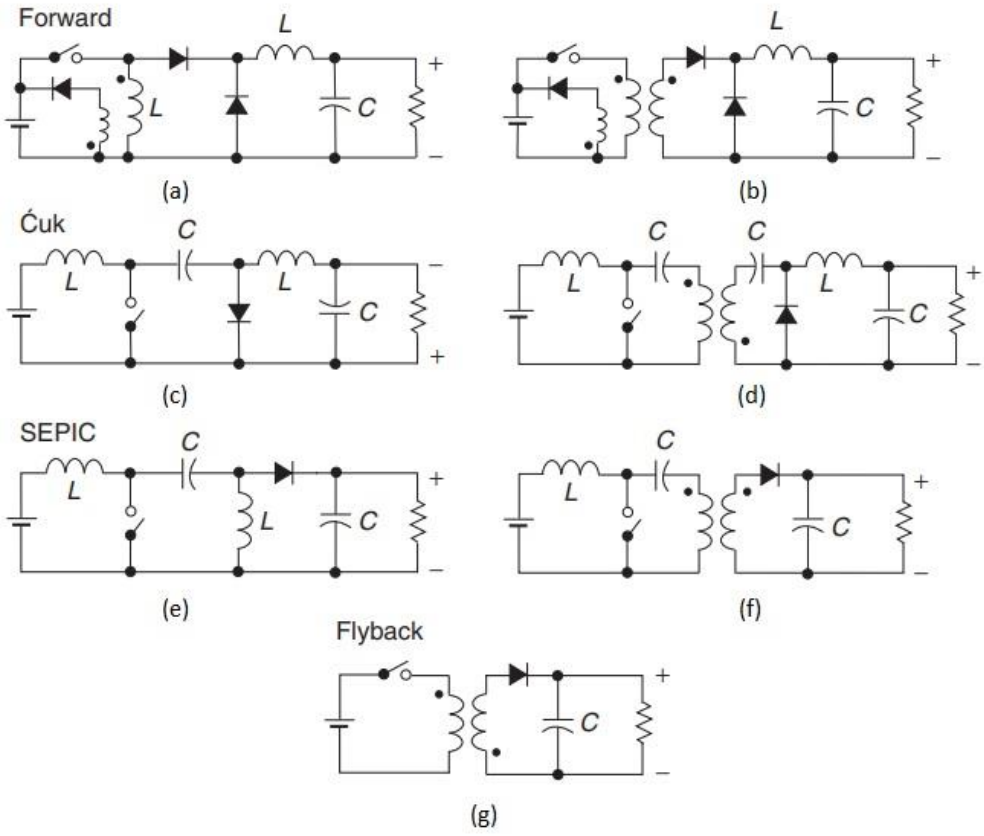

Figure 8. Different isolated and non-isolated converters [6].

Isolated converters are divided into forward, SEPIC, Ćuk and flyback, where forward, SEPIC and Ćuk can be made both isolated and non-isolated. Flyback is derived from a buck-boost, Ćuk converter is comparable with a boost-buck, SEPIC has similarities with a Ćuk converter and forward is a transformed version of a buck converter [6]. Figure 9 shows the different

converter family as non-isolated and isolated and table 2 compares differences between the converters.

Table 2. Comparison between different PWM converter topologies [6], [16], [17].

	Converters				
Features	Buck-boost	Ćuk	SEPIC	Flyback	forward
Output voltage polarity	Inverted	Inverted	Non-inverted	Non-inverted	Non-inverting
Input current	Pulsating	Pulsating	Non-pulsating	Non-pulsating	pulsating
Switch drive	Floated	Floated	Grounded	Grounded	Floated
Efficiency	Low	Medium	Medium	Low	Low
Cost	Medium due to float drive	Medium due to additional block capacitor	Medium due to block capacitor	Low due to grounded switch and no block capacitor	Medium due to float drive and a tertiary transformer winding

Comparison between these converters states that Buck-boost converter has discontinuous input current, high peak currents and poor transient response, while the Ćuk controller has low switching losses and higher efficiency than buck-boost when used as non-isolated dc-dc converters. SEPIC converter has lower efficiency than the Ćuk converter but the advantage of non-inverting output and grounded switch drives [16], [17].

Push-pull and half-bridge

Push-pull converter and half-bride converter are derived from buck converter topology [6]. Removing the diode bridge reduces the conduction loss and gives possibility of bidirectional power flow [13], [18]. Advantages of the push-pull converter is its gate-ground potential and utilization of its core. By referring both transistor-gates to ground makes it easier to drive the transistors and control the converter. The core of a push-pull converter is double-centre taped and exited from both directions, hence, well utilized and relatively small. However, due to small differences in circuit components, the transformer suffers from flux imbalance [6]. This will further lead to saturation of the transformer, a high current through the transistor and destruction of the transistor caused by over-heating. Avoiding this can be done with either a current sensor control that reduces the duty cycle of the heated transistor or using a larger transformer core to

avoid saturation. Because of transformer core imbalance, the push-pull is less attractive than the half bridge topology [6], [19].

The half-bridge converter avoids saturation of the core by blocking the dc component through the capacitor, and due to operation of the core in bipolar mode, the transformer core can be made relatively small [6]. Operating the transformer core in bipolar mode gives a cost advantage in single-transformer converters compare to a converter that operates the magnetic core in unipolar mode [6]. The disadvantage for the half-bridge converter is the need for an isolated driving circuit for the upper transistors. This is normally a small pulse transformer. The two transistors are arranged in totem and operated with 180° phase shift to avoid both to conduct simultaneously. If operated simultaneously, called cross-conduction, the transistors will be short circuited and further, destroying the transistors [6]. Figure 10a shows the push-pull converter topology and 10b shows the half-bridge topology.

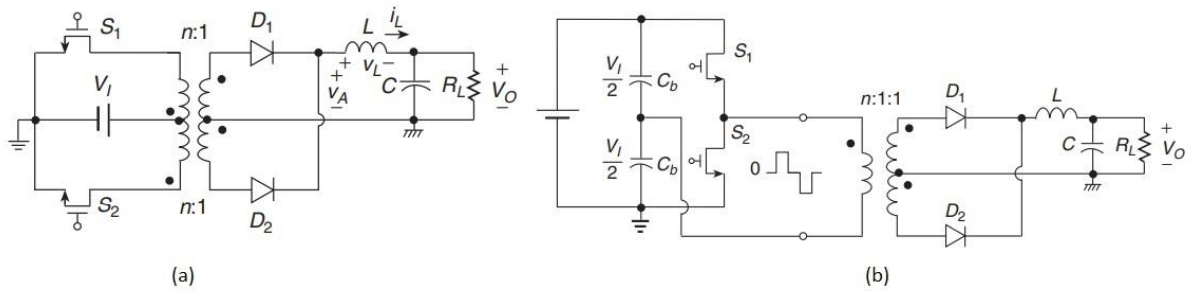

Figure 10. Push-pull and half bridge topology: (a) A push-pull converter. (b) A half-bridge converter topology [6].

2.2 Resonant converters

Resonant converters are a classification of converters in which switching strategies requires LC resonance. Resonant converters are classified into load-resonant tank, quasi-resonant, resonant-dc-link, and high-frequency- link integral-half-cycle converter as shown in figure 11 [14].

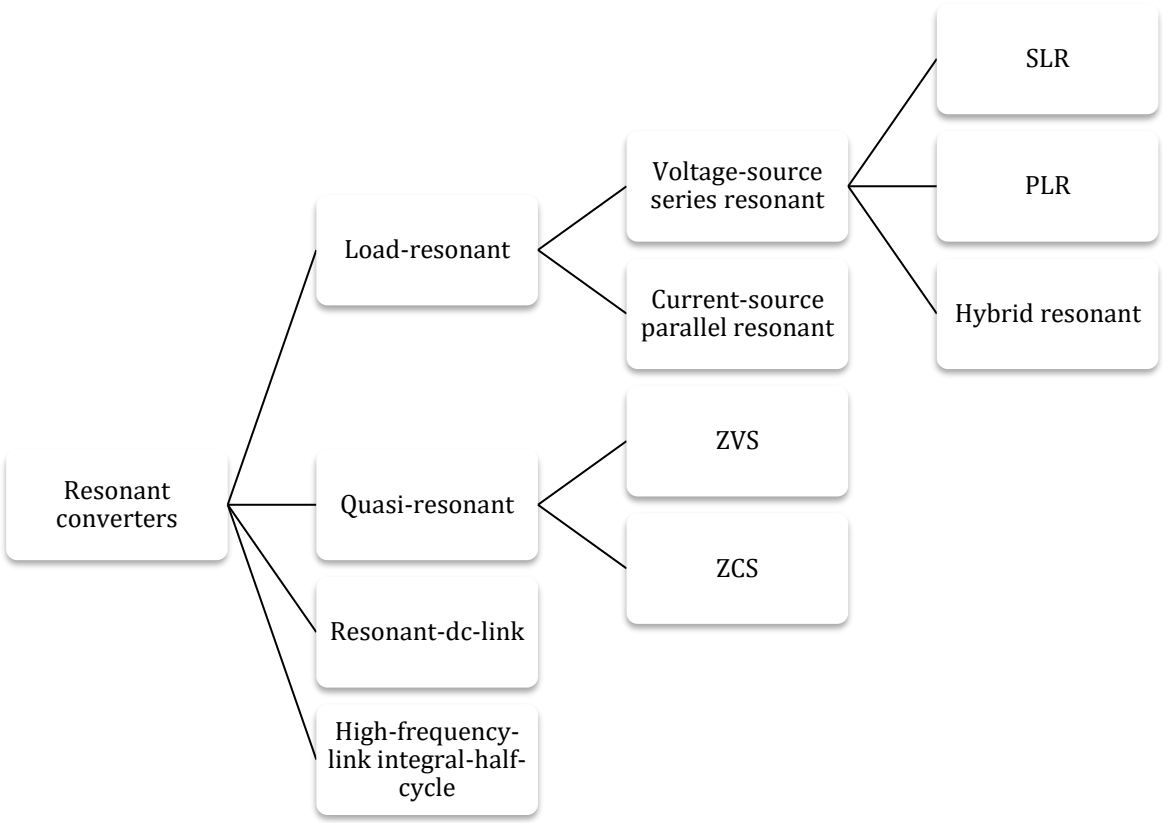

Figure 11. Resonant converters divided into Load-resonant converters, Quasi-resonant converters, Resonant dc-link converters and high-frequency-link integral-half-cycle converters.

Load-resonant

Load-resistant converters are further divided into voltage-source series resonant and current-source parallel resonant. This depend on if the source is modelled as a voltage source or a current source, as shown in figure 12 [20].

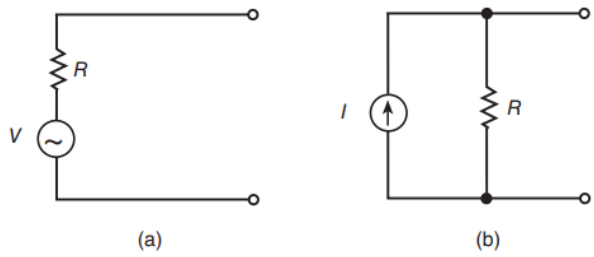

Figure 12. Voltage-source and current-source model [20].

These converters consist of an LC resonant tank in series-, parallel-, or through a hybrid circuit, where the output power flow is controlled by the resonant tank impedance. By adjusting the switching frequency, f_s, compared to the resonant frequency, f_0, the output power flow can be adjusted [14]. The resonant tank can also be named by its component, LC, LLC, or CCL, as shown in figure 13 [19].

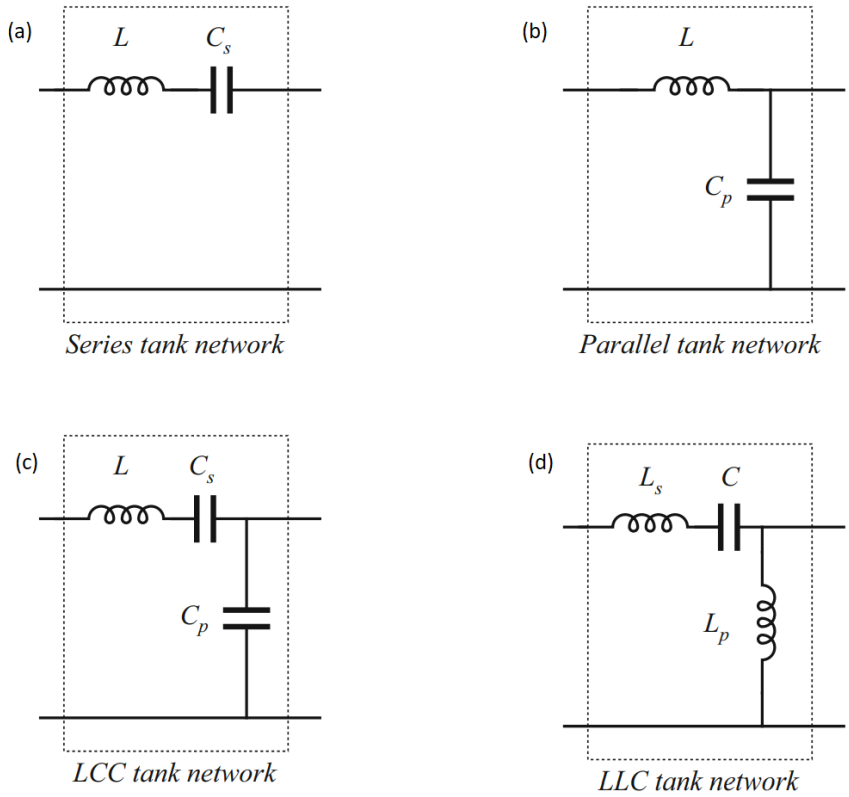

Figure 13. Series resonant tank, parallel resonant tank and hybrid resonant tank [19].

In load resonant converters, the LC tank is used to generate an oscillating load voltage and current that provides ZVS and/or ZCS [14]. In a series resonant circuit, the resonant tank appears to the load as a current source where an output filter capacitor maintains a constant voltage across the load. These converters have short circuit protection, and without a transformer, it works only as a step-down converter. The parallel resonant tank appears to the load as a voltage source making it suitable for multiple outlets. It works both as a step-up and step-down converter but does not have short circuit protection.

As figure 13a and 13b shows, the series and parallel resonant tank consist of two elements, L and C, which in general makes it easy to model. According to [21], these converters are considered as a three or four element converters when including the parasitic effect. The hybrid resonant tank, shown on figure 13c and 13d, has the advantages from both series and parallel

converters. This means inherent short circuit protection, converter acts as voltage source and capable of regulating the no-load voltage [14]. Further study on a three elements resonant circuits can be found in [22]

Quasi-resonant

Quasi-resonant converter, also called resonant-switching converter, use a conventional PWM with an auxiliary LC circuit that shapes the current and/or voltage across the switch to achieve ZVS or ZCS [14]. Figure 14a shows a buck, figure 14b shows a boost converter and figure 14c shows a buck-boost converter as a ZVS quasi-resonant topology. Topologies for ZCS quasi-resonant converters can be find in [6]. The ZVS resonant circuit is obtained by adding a resonant capacitor, C_r, in parallel with the switch and a resonant inductor, L_r, in series with the transistor and resonant capacitor. The transistor output capacitance is absorbed into the resonant capacitor and the diode inductance is absorbed into the resonant inductor[6]. A further elaboration about quasi-resonant converter technologies can be found in [23], [24]. Paper [25] shows a boost converter achieved higher efficiency at high output power using boost converter with ZVS auxiliary circuit compared to a conventional PWM technics.

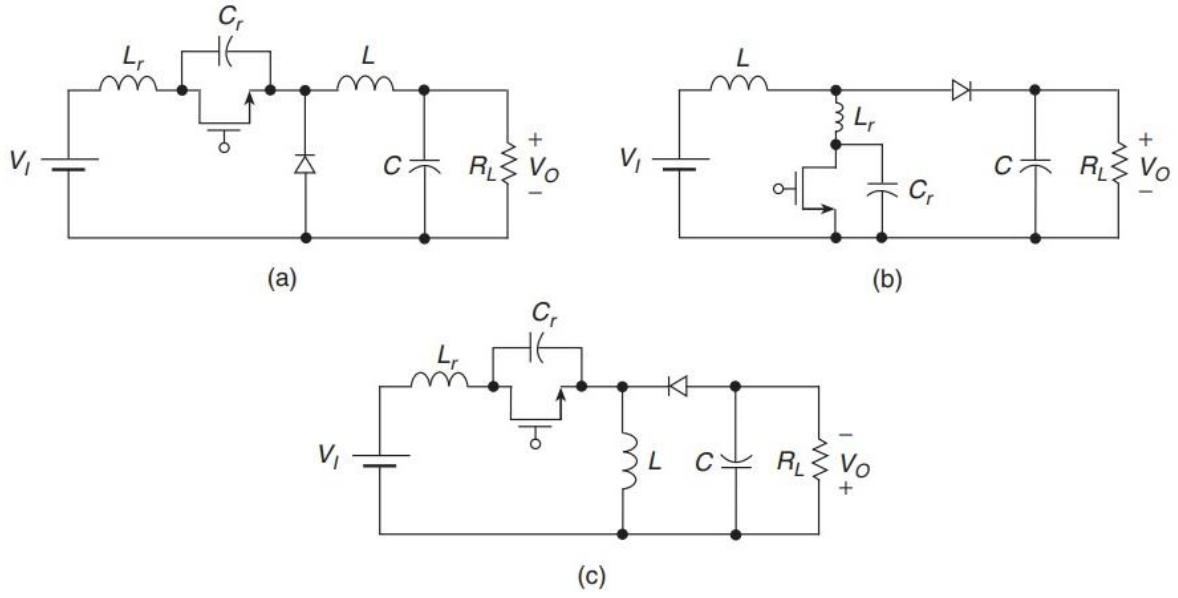

Figure 14. Quasi-resonant buck, boost and buck-boost converters: (a) Quasi-resonant buck converter. (b) Quasi-resonant Boost converter. (c) Quasi-resonant Buck-boost converter topology [6].

Resonant DC-link

Resonant-dc-link converters resonates between the input and the switching transistor which gives ZVS with voltage stress across the switch higher than the input average dc-voltage [14]. The converter can be used as DC-AC single-phase but has a most potential in DC-AC three

phase or three-phase AC to three-phase AC [26]. Figure 15a shows a conventional PWM DC-AC converter and 15b shows a resonant DC-link DC-AC converter. These converters use dc input voltage and provides an ac output. The benefits of using DC-link converter are high switching frequency, eliminating of switching loss, good dynamic and transient response, simple control and low harmonics on ac side [26]. Paper [27] shows that a DC-link converter can be used as three-phase AC to three-phase AC with half the number of switches compared to a conventional PWM converter.

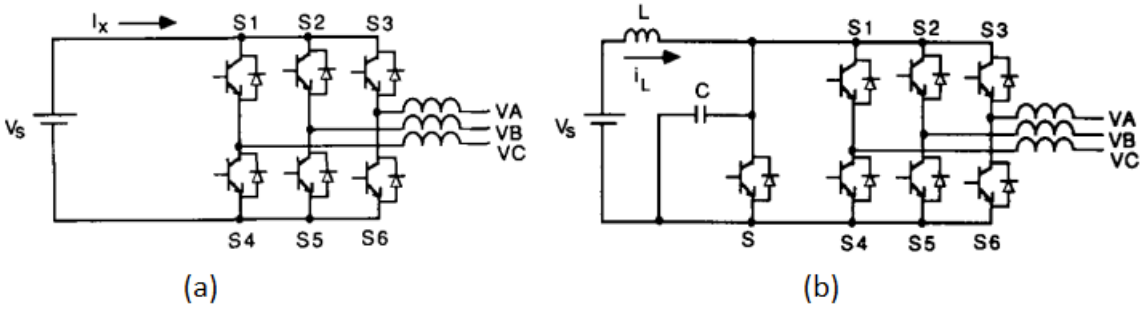

Figure 15. Conventional PWM and Resonant DC-link converter: (a) Conventional PWM converter. (b) Resonant DC-link converter topology [26].

High-frequency link integral-half-cycle

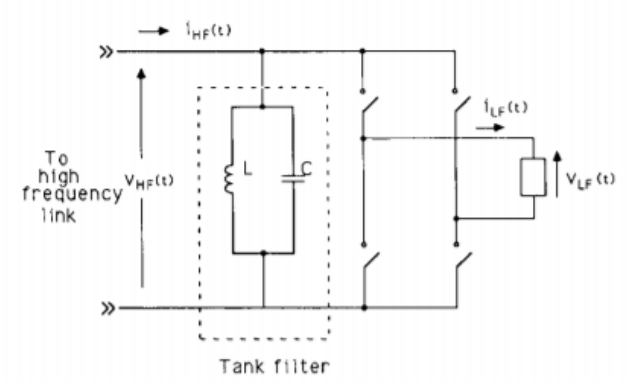

Figure 16. High-frequency link integral-half-cycle converter topology [28]

High-frequency-link integral-half-cycle converters are an alternative to the Resonant DC-link converter [28]. It uses a single-phase high-frequency input voltage, and the output can be single-phase or three-phase low-frequency AC or a DC voltage. This converter uses bidirectional switches that operates on zero-crossing of the input voltage, which gives the converter inherently possibility of bidirectional power flow [14], [28]. Figure 16 shows a single-phased high-frequency link integral-half-cycle converter.

3 Topology selection

The suggested topologies are based on a Class-E zero voltage switching (ZVS) circuit. Class-E resonant converter has been under research and development for a continuously increasing usage. [6], [29]–[31]. The given name comes from radio frequency amplifier classification, where Class-A to Class-C refers to amplifiers where the transistor acts as a current source [29]. Class-A operate the transistor within the linear region, Class-B operates the transistor at the boundary between cut-off region and active region. In contrast, Class-C operate the transistor in cut-off region [20]. Class-B and Class-C are based on parallel resonant tank circuits, Class D-can have both series and parallel resonant circuits, and Class-E is based on series resonant circuits [20], [31].

3.1 Class-D

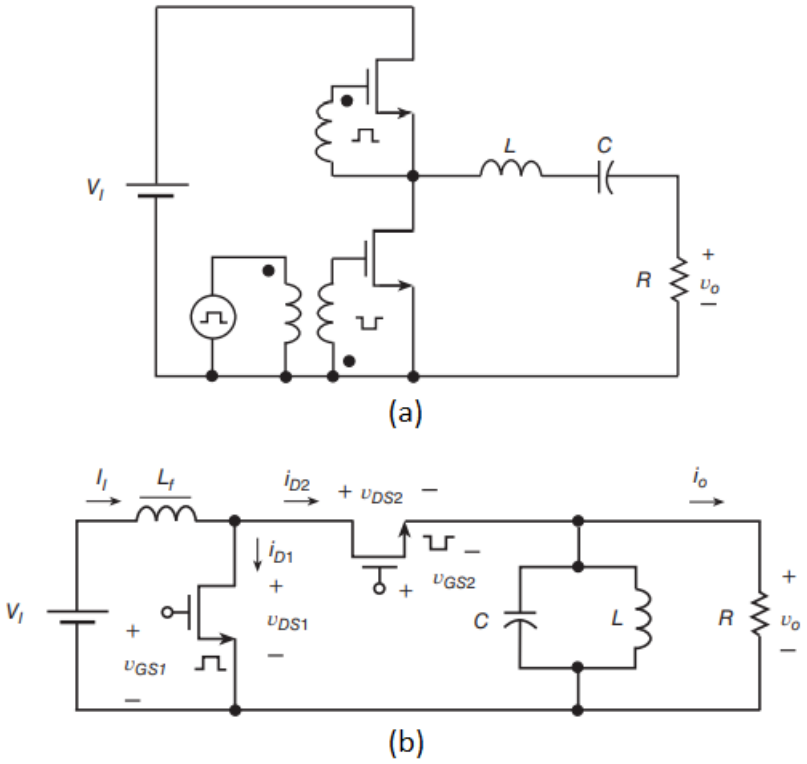

Figure 17. Class-D converter modeled as a voltage source series resonant circuit and a current source parallel resonant [20].

Class-D is used in many DC-DC or DC-AC applications, such as LED drivers, induction heating, etc. When used in DC-DC applications it has rectifying effect at the load [20]. Class-D converters can be either voltage source or current source. The voltage source employs a series-resonant circuit, and the current source employs a parallel-resonant circuit. Figure 17

shows the difference between the Class-D voltage source and Class-D current source circuit [20].

An advantage of the Class-D voltage source amplifier is the low voltage across each transistor, equal to the supply voltage. However, it has a disadvantage which is difficulty to drive the upper MOSFET. The figure17a shows that a non-inverting output of the transformer drives the upper MOSFET, while the lower is driven by an inverted output [20].

3.2 Class-E

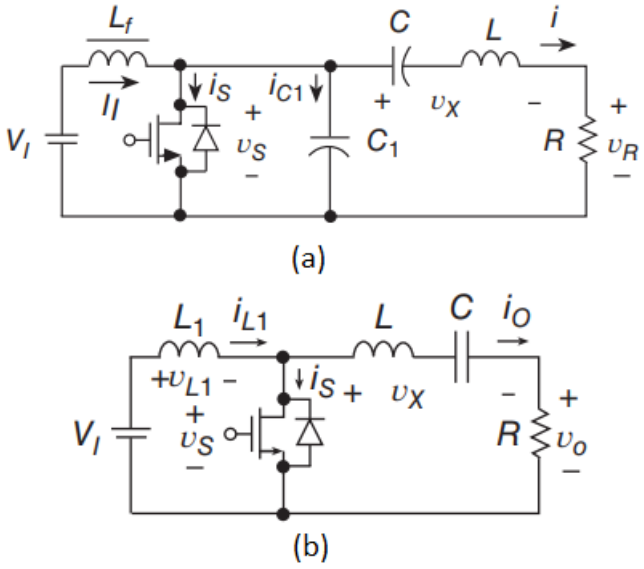

Figure 18. Class-E ZVS circuit and Class-E ZCS circuit [20].

Class-E converters has high-efficiency operation at higher frequencies than Class-D circuits. There are two types of Class-E converters, zero voltage switching (ZVS) and zero current switching (ZCS). The Class-E ZVS circuit operates the transistor when the voltage across it is zero volt. The Class-E ZCS turns off the transistor at zero current but turns on the switch at non-zero values which dissipate the energy stored in the output parasitic capacitance and reduce the efficiency. This makes the ZVS circuit more efficient than the ZCS circuit, and according to [20], [31], the Class-E ZVS power amplifier is the most efficient known so far. Figure 18a shows a Class-E ZVS circuit and figure 18b shows a Class-E ZCS circuit.

The two differences in the schematic of these circuits are the missing shunt capacitor in the ZCS circuit and the emphasizes on the inductor and capacitor. The ZVS circuit has an inductive series resonant tank and operates in the inductive region meaning it switches on and off the transistor above its resonance frequency. The ZCS circuit has a capacitive series resonant tank

and operates in the capacitive region meaning that it switches beneath the resonance frequency [20].

The disadvantages of a Class-E ZVS resonant converter are the high switching stress across the transistor and the need for a wide range of frequency to regulate the output voltage [3]. According to [14], the average voltage across the transistor of a Class-E converter is equal to the RMS value of the connected grid voltage. The high voltage stress across the switch can be reduced by different techniques. These techniques are placing a Zener diode across either the switch or inductor, or placing a transformer with a diode in series in parallel with the input voltage [32]. Placing a Zener diode in parallel is done in [33] and in parallel with the inductor in [34], where the power loss was reduced with two-thirds compared with placing the Zener diode across the switch. A transformer with a diode placed in parallel to the input voltage gave according to [35] ringing in the switch voltage waveform due to leakage inductance in the transformer.

Operation of Class E

The converter's ZVS capability is depending on the load resistance. If the connected resistance is at optimum value, R_{opt}, the transistor operates at optimum operation, meaning that it can both achieve ZVS and zero derivative switching (ZDS). In these cases, the transistor switches when the slope of the current or voltage is zero and gradually increases [20], [31].

If the connected resistor is lower than the optimum resistance, $R_i \leq R_{opt}$, the transistor operates at suboptimum operation. When the Class-E ZVS converter is operating in suboptimum operation, it achieves ZVS but not ZDS, which leading to a current through the body diode turning on the switch automatically. This leads to an on-duty cycle less or equal to the set duty cycle, $D_{on} \leq D$. If the connected resistance is higher than the optimum resistance, $R_i \geq R_{opt}$, the voltage across the transistor is higher than zero, and ZVS cannot be achieved [20], [31]. This problem can be avoided by using an inductive impedance inverter, described in [32], [36]. Class E ZVS converter operating outside of the ZVS and ZDS switching condition is described in [37]

If the Class E ZCS operates in optimum operation, menaning that ZDS is fulfilled, the voltage across the transistor is zero in the swithcing moment. This results in no stored energy in the parasitic capacitance and further no energy loss during swhitching. If the Class-E ZCS converter operates in suboptimum operation, it fulfills ZCS, but not ZDS, it will have the body diode conduct if the transistor is turned off. If ZCS is not fulfilled, the transistor will turn off at

non-zero current and it will act as a current source with a fall time. The fall time will overlap with the rising voltage and generate a power loss. In addition, the transistor will have dangerous voltage spikes at the output [20], [31].

3.3 Suggested converters

Throughout this project there will be suggested two circuits used for PFC where both is based on a resonant Class-E converter with ZVS. These two circuits are shown on figure 19.

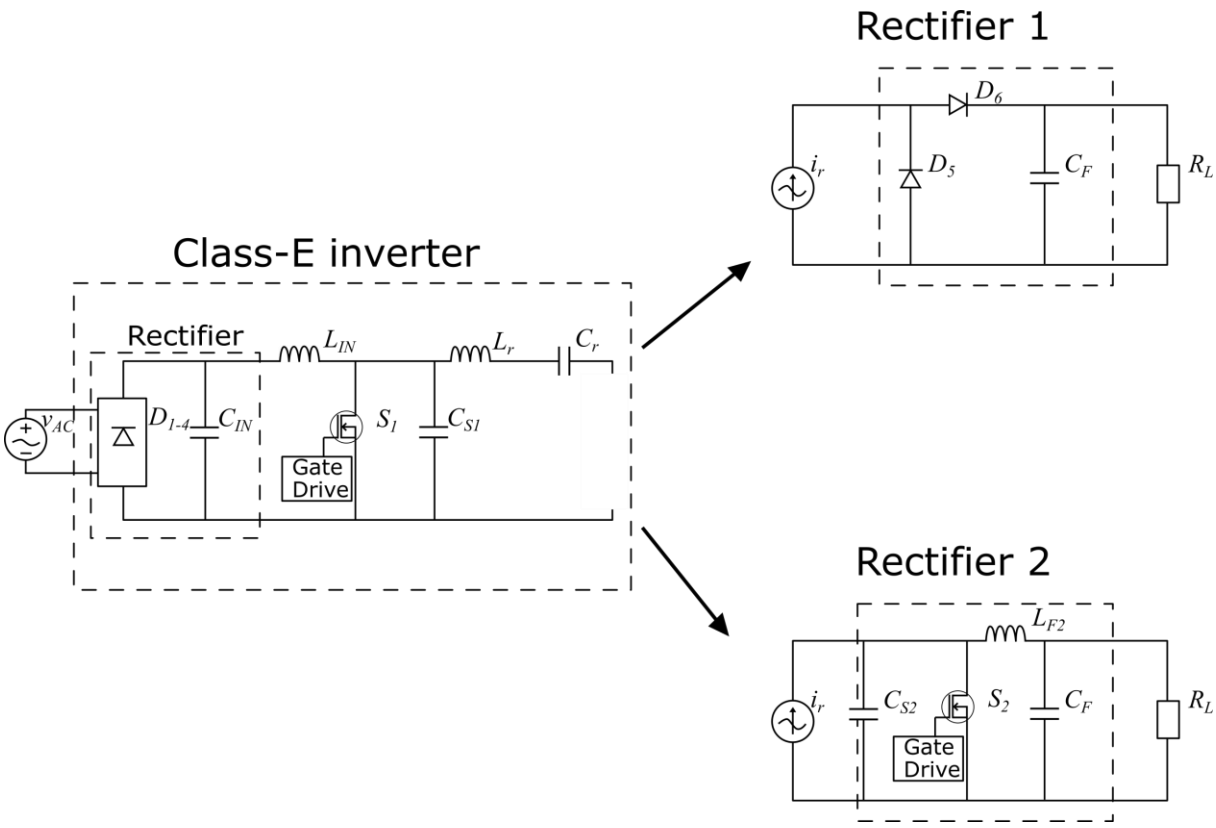

Figure 19. Class-E inverter with suggested converter 1 and 2.

The Class-E converter is an inverter with an input of DC and output of AC, also known as a DC-AC inverter [31]. When designing an application with alternating current as input and direct current as output, a rectifier is needed. In this case, the Class-E converter has a diode bridge rectifier at the input, and a rectifier circuit on the output. The first rectifier circuit is a current driven rectifier using diodes for rectification and the second rectifier circuit is a mirroring of the Class-E inverter. The first proposed converter is in [2] suggested as a PFC converter which is redesigned here to operate at 1 MHz. The second converter is in [3] proposed as a high-efficient DC-DC converter.

4 Modelling

This chapter present the mathematical model of the two suggested topologies. Class-E inverters are designed according to the following assumption:

Assumptions

- All components are assumed to be ideal.
- The analysis is done as a state-space analysis.
- The first-order analysis is considered, meaning the total harmonic content of the circuit is close to zero.
- The switching frequency is higher than the resonant frequency. Hence, the inverter will switch in the inductive region.
- The loaded quality factor should be high enough to have a sinusoidal current.

4.1 Class-E converter

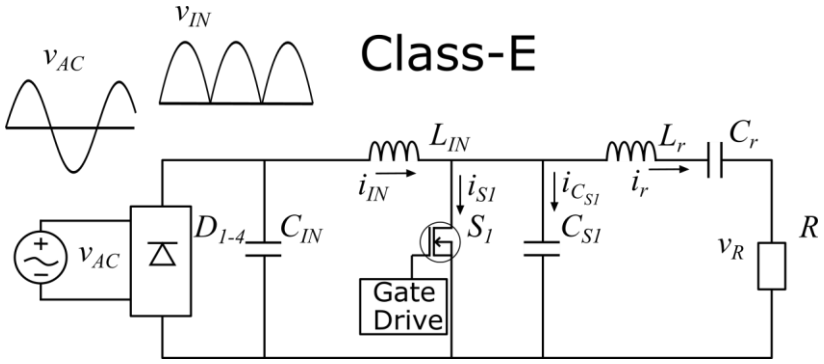

Figure 20. Class-E converter

Figure 20 shows the Class-E converter with the waveform of the applied voltage. The following mathematical model is derived on from the waveforms of the inverter [31]. The figure shows that the input voltage is as an alternating voltage passed through a diode bridge. This gives an input voltage expressed as:

$$v_{IN} = V_{AC}|\sin(\omega_{IN}t)| \tag{4,1}$$

Where $|\sin(\omega_{IN}\, t)| = |\sin(\omega_{AC}\, t)|$. The first-order analysis gives the following input current:

$$i_{IN} = I_{IN}|\sin(\omega_{IN}t)| \tag{4,2}$$

Where I_{IN} is the amplitude of the current through the input inductor and ω_{IN} is the angular frequency of the input current. The minimum value of input inductor is calculated from following relationship [31], [38]:

$$L_F = 2\left(\frac{\pi^2}{4} + 1\right)\frac{R}{f_r} \tag{4,3}$$

Using equation (4,2) can model the inverter as a current source equivalent as shown in figure 21 [14], [20].

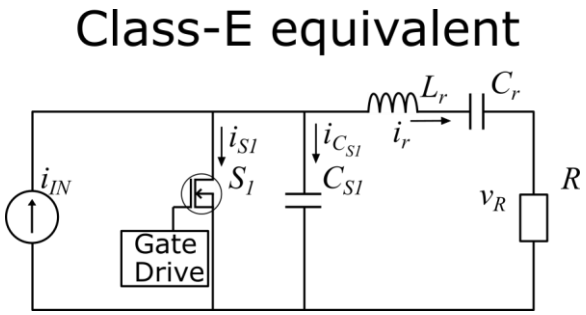

Figure 21. Class-E current source equivalent. [14], [20]

Evaluation of the circuit according to Kirchhoff's current law gives:

$$i_{S1} + i_{C_{S1}} = I_{IN}|\sin(\omega_{IN}t)| - I_r \sin(\omega_{S1} + \phi_1) \tag{4,4}$$

Where I_r is the amplitude of current in the resonant tank current, ω_{S1} is the switching frequency and ϕ_1 is the initial phase of the current i_r. The current through the switch and voltage across are found by:

$$i_{S1}(\omega_{S1}t) = \begin{Bmatrix} I_{IN}\sin(\omega_{IN}t) - I_r * \sin(\omega_{S1}t + \phi_1) \\ 0 \end{Bmatrix}, \quad \begin{matrix} 0 \le \omega_{S1}t \le 2\pi D_1 \\ 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{matrix} \tag{4,5}$$

Where D_1 is the duty cycle of switch 1. Using (4,5), the voltage across the capacitor and transistor by:

$$v_{S1}(\omega_{S1}t) = \frac{1}{\omega_{S1}C_{S1}}\int_{2\pi D_1}^{\omega_{S1}t} i_{C_{S1}} d(\omega t)$$

$$= \begin{Bmatrix} \frac{1}{\omega_{S1}C_{S1}} \begin{bmatrix} 0 \\ I_{IN}\sin(\omega_{IN}t)\,(\omega t - 2\pi D_1) \\ +I_r(\cos(\omega_{S1}t + \phi_1) - \cos(2\pi D_1 + \phi_1)) \end{bmatrix}, & \begin{matrix} 0 \le \omega_{S1}t \le 2\pi D_1 \\ 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{matrix} \end{Bmatrix} \tag{4,6}$$

Substituting (A,8) and (A,9) into (4,2) and (4,4) gives the maximum current and voltage through the switch:

$$\frac{i_{S1,max}}{I_{IN}\sin(\omega_{IN}t)} = \begin{Bmatrix} 1 - \frac{2\pi(1-D_1)\sin(\omega_{S1}t_{imax} + \phi_1)}{\cos(2\pi D_1 + \phi_1) - \cos\phi_1}, & \begin{matrix} 0 \le \omega_{S1}t \le 2\pi D_1 \\ 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{matrix} \\ 0 \end{Bmatrix} \tag{4,7}$$

$$\frac{v_{S1,max}}{V_{IN}} = \begin{cases} 0 & 0 \le \omega_{S1} t \le 2\pi D_1 \\ \dfrac{\tan(\pi D_1 + \phi_1) * \sin \pi D_1}{(1-D_1)[\pi(1-D_1)\cos \pi D_1 + \sin \pi D_1]} * \dfrac{\left[\left(\omega_{S1} t_{v,max} - 2\pi D_1\right) + 2\pi D_1 (1-D_1)\left[\cos\left(\omega_{S1} t_{v,max} + \phi_1\right)\right]\right]}{\cos(2\pi D_1 + \phi_1) - \cos \phi_1}, & 2\pi D_1 \le \omega_{S1} t \le 2\pi \end{cases} \quad (4,8)$$

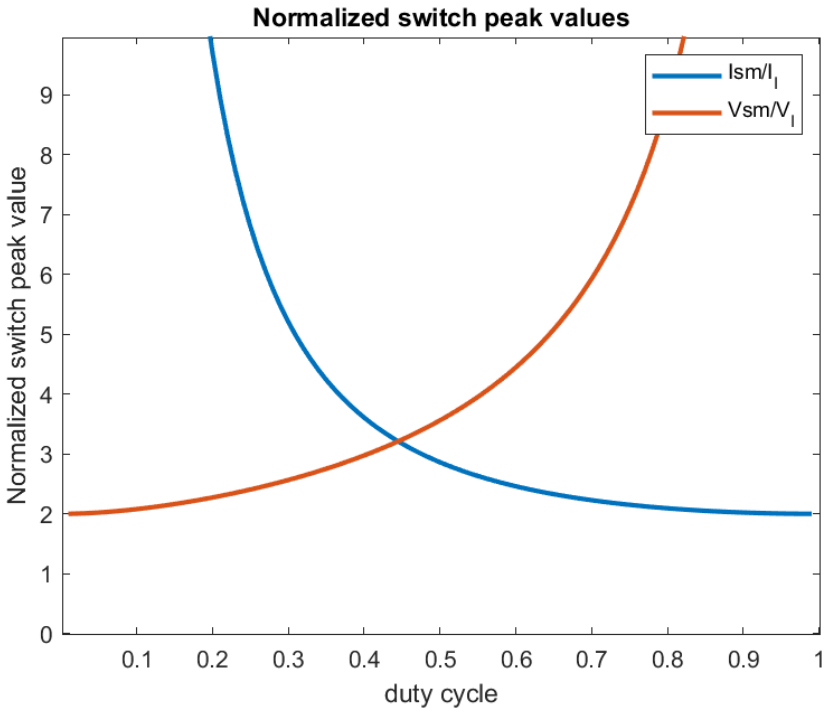

Figure 22. Normalized switch peak values

Plotting (4,7) and (4,8) in figure 22 visualize the maximum current through and voltage across the transistor. The current and voltage stress across the switch is 3.24 times the input waveform at duty cycle 0.45. The result matches the ones for a DA-AC inverter reported in [31]. Further, the output voltage and power flow can be found by:

$$V_R = \frac{1}{\pi} \int_{2\pi D_1}^{2\pi} v_S \sin(\omega_{S1} t + \phi_1)\, d(\omega_{S1} t) = -\frac{2 \sin(\pi D_1) \sin(\pi D_1 + \phi_1)}{\pi(1-D_1)} V_{IN} \quad (4,9)$$

$$P_{out} = \frac{V_R^2}{2R} = \frac{2 \sin^2 \pi D_1 \sin^2(\pi D_1 + \phi_1) V_{IN}^2}{\pi^2 (1-D_1)^2 R} \quad (4,10)$$

Where (A,5) shows that ϕ_1 is a function of D_1, hence V_R is a function of D_1 for the given frequency. Further, the shunt capacitor is found by:

$$C_{S1} = \frac{2\sin(\pi D)\sin(\pi D + \varphi_1)\cos(\pi D + \varphi_1)[(1 - D_1)\pi\cos(\pi D_1) + \sin(\pi D_1)]}{\pi^2(1 - D_1)\omega_{S1}R} \quad (4,11)$$

Since the series resonant tank is inductive, the reactance of the inductor is larger than the reactance of the capacitance, $X_L > X_{Cr}$. This means that the reactance of the inductor can be divided into two parts, $L = L_a + L_b$, where $X_C = X_{La}$.

The inductive equivalent of the resonant tank circuit is found by:

$$L_b = \frac{\begin{array}{c}2(1 - D_1)^2\pi^2 - 1 + 2\cos(\varphi)\cos(2\pi D_1 + \varphi_1) - \\ \cos(2(\pi D_1 + \varphi_1))[\cos(2\pi D_1) - \pi(1 - D_1)\sin(2\pi D_1)]\end{array}}{4\sin(\pi D_1)\cos(\pi D_1 + \varphi_1)sin(\pi D_1 + \varphi_1)[(1 - D_1)\pi\cos(\pi D_1) + \sin(\pi D_1)]} * \frac{R}{\omega_{S1}} \quad (4,12)$$

As the Q_L is a chosen to be high enough to ensure a pure sinewave, the inductor can be found from:

$$L = \frac{Q_L * R}{\omega} \quad (4,13)$$

Where Q_L is the loaded quality factor. Paper [3] stated that the loaded quality factor when the switch is on should be higher than or equal than five. A high quality factor results in more energy resonating in the resonant tank compare to a low quality factor. Energy resonating in the tank gives energy dissipated through the parasitic resistance of the inductor and capacitor compare to a low quality factor [32].

Further, the resonant capacitor has relationship:

$$\frac{1}{\omega C_r} = \omega L_a \quad (4,14)$$

4.2 The first suggested Class-E based converter

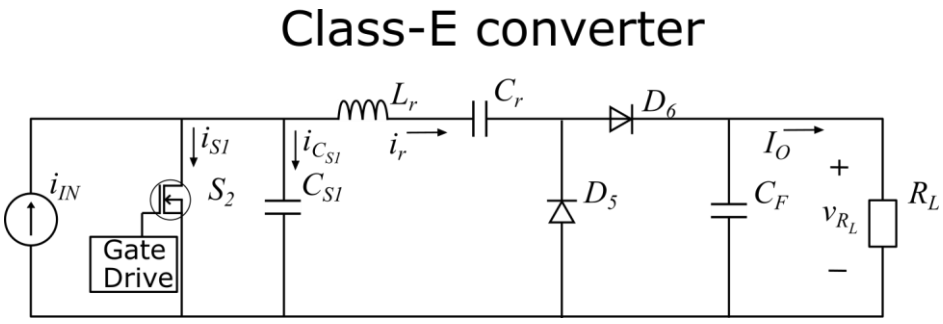

Figure 23. Class-E converter proposal 1

The first PFC converter suggested topology is a Class-E converter with a Class-D rectifier in series, as shown on figure 23. The following circuit and its mathematical model is based on [2], [31]. The resonant current, i_r, is found in (A,2) in the appendix A. The duty cycle of each conducting diode is 0.5, and the following current remains:

$$i_{D6} = \begin{cases} i_r, & 0 \leq \omega_{S1} t \leq \pi \\ 0, & \pi \leq \omega_{S1} t \leq 2\pi \end{cases} \tag{4,15}$$

Further, the output current is found by:

$$I_O = \frac{1}{2\pi} \int_0^{\pi} i_{D6} d(\omega t) = \frac{2I_{IN} \sin(\omega_{IN} t)\,(1 - D_1)}{\cos(2\pi D_1 + \phi_1) - \cos(\phi_1)} \tag{4,16}$$

The DC output current, I_O, is proportional to the resonant current by following relationship:

$$K = \frac{I_O}{I_r} = \frac{\sqrt{2}}{\pi} \tag{4,17}$$

Where I_r is the Amplitude of the resonant current i_r. Substituting (A,2) into (4,17) gives following current gain:

$$|G_I| = \frac{I_O}{I_r} * \frac{I_r}{I_{IN}} = \frac{2\sqrt{2}(1 - D_1)}{\cos(2\pi D_1 + \phi_1) - \cos\phi_1} \tag{4,18}$$

Plotting (4,18) in figure 24 visualize the current gain as a function of duty cycle. From appendix, (A,5) shows that ϕ_1 is a function of duty cycle. Thus, current gain is only depending on duty cycle.

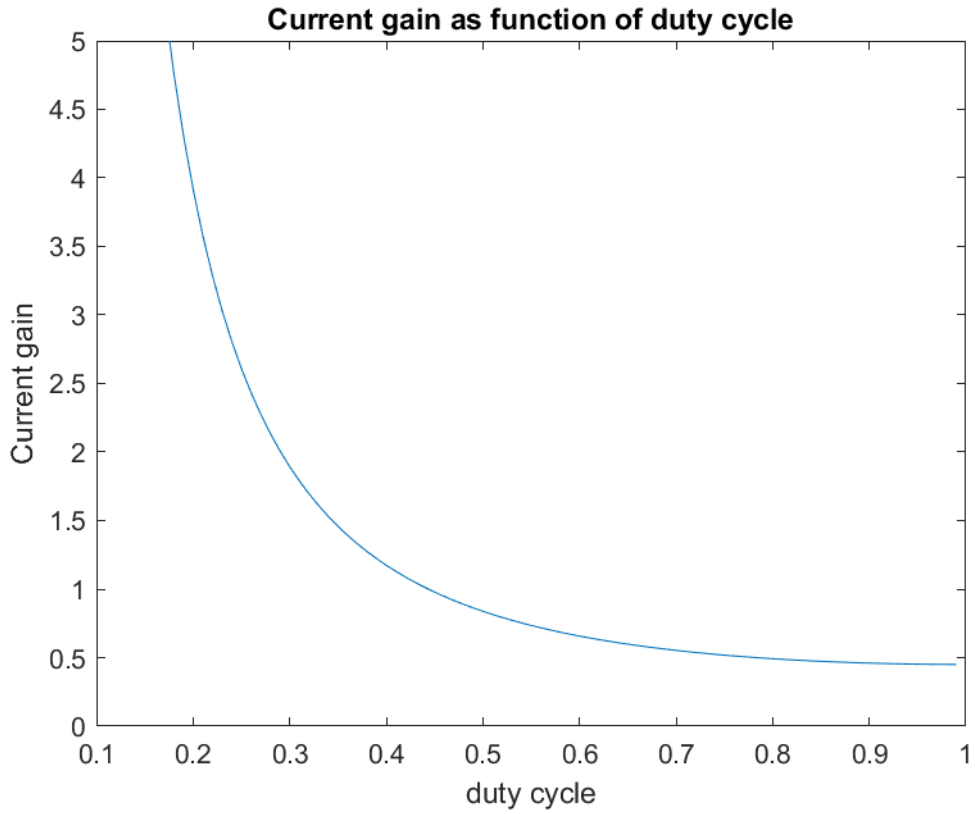

Figure 24. Current gain through the proposed converter 1.

Reflecting the resistance, R, from the Class-E inverter on figure 20, to the output of the rectifier, R_L, has relationship:

$$R_L = \frac{\pi^2 R}{2} \tag{4,19}$$

Hence, the output voltage is:

$$V_O = I_O * R_L \tag{4,20}$$

Generating a output DC-DC voltage with a ripple equal or lower than 2% is done by adding a filter capacitor with size [39], [40]:

$$C_F \geq \frac{P_{out}}{0.04 * V_{C_F}^2 * \omega_{IN} * \eta} \tag{4,21}$$

Where the ripple of the voltage across the capacitor has doble-the-input frequency [39].

4.3 The second suggested Class-E based converter

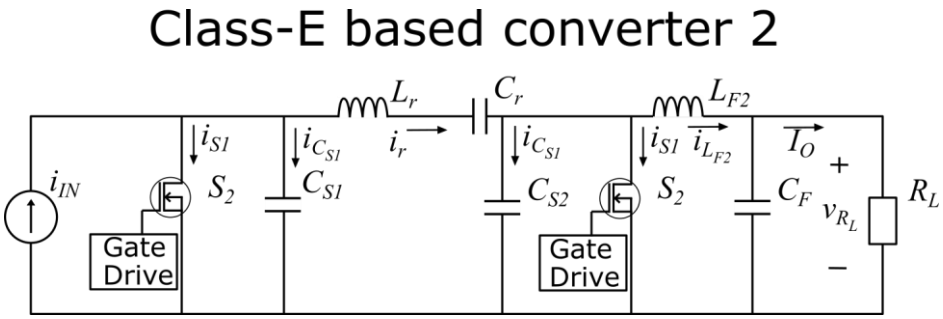

Figure 25. Class-E based converter 2.

The second suggested converter for PFC is a Class-E converter in series with mirrored Class-E converter. The circuit, shown in the figure 25, is based on [3], [38]. From (A,2), the capacitor current i_{CS2} has following relationship.

$$i_{C_{S2}} = \begin{cases} i_r - I_{L_{F2}}\left|\sin\left(\omega_{L_{F2}}t\right)\right|, & 0 \le \omega_{S2}t \le 2\pi D_2 \\ 0 & 2\pi D_2 \le \omega_{S2}t \le 2\pi \end{cases} \tag{4,22}$$

Following mathematical relationship holds for this circuit,

$$v_{S2}(\omega_{S2}t) = \frac{1}{\omega_{S2}C_{S2}}\int_{2\pi D_2}^{\omega_{S2}t} i_{C_{S2}}\, d(\omega_{S2}t)$$

$$= \begin{cases} 0 & 0 \le \omega_{S2}t \le 2\pi D_2 \\ \dfrac{1}{\omega_{S2}C_{S2}}\left[\dfrac{I_{IN}\sin(\omega_{IN}t)2\pi(1-D_1)(\cos(2\pi D_2+\phi_2) - \cos(\omega_{S2}t+\phi_2))}{\cos(2\pi D_1+\phi_1)-\cos(\phi_1)}\right] & 2\pi D_2 \le \omega_{S2}t \le 2\pi \\ -I_O\sin(\omega_{L_{F2}}t)(\omega_{S2t}t - 2\pi D_2) & \end{cases} \tag{4,23}$$

Substituting the ZVS condition, $v_{C_{S2}}(2\pi) = 0$, into (4,23) gives the following relationship between the input current and the output current.

$$I_{IN} = \frac{I_O\sin(\omega_{L_{F2}}t)(1-D_2)(\cos(2\pi D_1+\phi_1)-\cos\phi_1)}{\sin(\omega_{IN}t)(1-D_1)(\cos(2\pi D_2+\phi_2)-\cos\phi_2} \tag{4,24}$$

Assuming $\sin(\omega_{IN}t) \approx \sin(\omega_{L_{F2}}t)$ gives following relationship of the gain:

$$|G_I| = \frac{I_O}{I_{IN}} = \frac{(1-D_1)(\cos(2\pi D_2+\phi_2)-\cos\phi_2)}{(1-D_2)(\cos(2\pi D_1+\phi_1)-\cos\phi_1)} \tag{4,25}$$

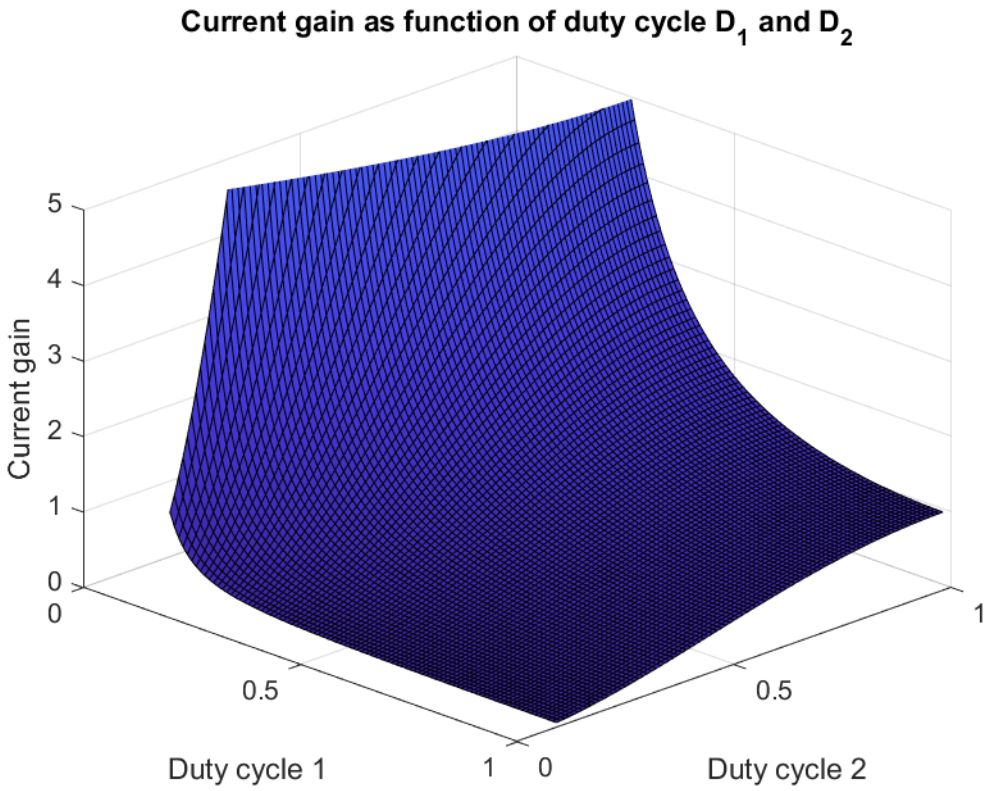

Figure 26. Current gain for the second suggested converter.

Plotting (4,25) in figure 26 visualizes the current gain through the converter as a function of duty cycle 1 and duty cycle 2.

Substituting (4,24) into (4,23) gives the voltage across the switch:

$$v_{S2}(\omega_{S2}t) = \frac{I_O}{\omega_{S2}C_{S2}}\left\{\begin{array}{c}\frac{2\pi(1-D_2)(\cos(2\pi D_2+\phi_2)-\cos(\omega_{S2}+\phi_2))}{(\cos(2\pi D_2+\phi_2)-\cos\phi_2} \\ -I_O(\omega_{S2}t-2\pi D_2)\end{array}\right\} \qquad (4,26)$$

5 Design

This chapter present the design of the two suggested Class-E PFC topologies, the resonant inductor design and PCB design. The designing is done in Altium Designer and CircuitCam. The Altium Designer is a designing program for PCBs to create a Gerber-file for printing the PCB. Printing the PCB needs in addition CircuitCam to produce an LMD-file for manufacturing.

5.1 Converter design

The converters are based on a Class-E with parameters listed in table 3.

Table 3. Parameter used in converter design.

Parameters	Specifications
Input voltage, V_{IN}	240 V
Line frequency, f_{IN}	50 Hz
Power, P	300 W
Resonant frequency, f_r	0,9 MHz
Switching frequency, fs	1 MHz
Quality factor, Q_L	6
Duty cycle, D_1	0.45
Duty cycle 2 (rectifier 2), D_2	0.3

These parameters are used to calculate the component values listed in table 4. Using a resonant frequency lower than the switching frequency gives switching in inductive region.

Table 4. Calculated component values.

Passive components	Calculated value
Input capacitor, C_{IN}	[32]
Load resistance, R_L	401 Ω
Resonant inductor, L_r	86,3 µH
Shunt capacitor, C_{S1}	476 pF
Resonant capacitor, C_r	471 pF
Choke inductor, L_{IN}	626 µH
Filter capacitor, C_F	609µF

The bill of material used for both converters is found in table 5.

Table 5. Bill of material for suggested converters.

Bill of material				
Symbol	**Component**	**Description**	**Part number**	**Supplier**
D1 - D4	Diode bridge	GBU8M-E3/51	300-48-126	Elfa

S	MOSFET	SCT2750NYTB	2772413	Farnell
C_{IN}	Capacitor	ECA2WHG010	9693394	Farnell
L_{IN}, L_{OUT}	inductor	On storage	On storage	On storage
C_S	Shunt capasitor	C1206C221JGGACTU	2676440	Farnell
L_r	Ferrite core	T130-2	158-74-094	Elfa
L_r	Litz Wire	CLI 200/120	155-16-562	Elfa
C_r	Capacitor	C1812C471JZGACAUTO	2834661	Farnell
D5, D6	Schottky diode	C6D04065A	3290064	Farnell
C_F	Capacitor	ALC70A561DF450	2950244	Farnell

5.2 Inductor design

The resonant inductor for the circuit is designed according to [41] with an toroidal core from Micrometals, T130-2 core, and Litz wire CLI 200/120 for wiring. The parameters used through the design is given in table 6.

Table 6. Parameter used through designing of resonant inductor.

Parameters	Specifications
Resonant inductor, L_r	86,3 µH
Peak voltage, V_{Lmaks}	1700 V
Frequency, f	1 MHz
Power P	300 W
Expected resonant current, I_{RMS}	2,8 A
Loaded quality factor, Q_L	6

Table 7 gives the calculated and measured values for resonant inductors. The mathematical relationship used through the design is found in appendix B.

Table 7. Calculated and measured parameters for the resonant inductors.

Inductor parameter	Calculated	Measured
Inductance, L	86.6 µH	86.5 µH
Numbers of turns, N	89 turns	89 turns
Length of Litz Wire, l_T	4.21 m	4.2 m
Magnetic flux density, B	437 Gauss	N.A
Core Loss per cubic centimeter, P_{CORE}	2.38 W/cm^3	N.A
Resistance Litz wire, R_L	0.1 Ω	0.2 Ω
Parasitic resistance	N.A	4 Ω

5.3 PCB design

The converters are designed in Altium Designer and produced at UiT campus Narvik. Figure 39 shows a picture of the proposed converters with a protective cover. In both printed circuit boards (PCBs), the through-hole component is mounted on the bottom side of the board to minimise the size and further increase the power density.

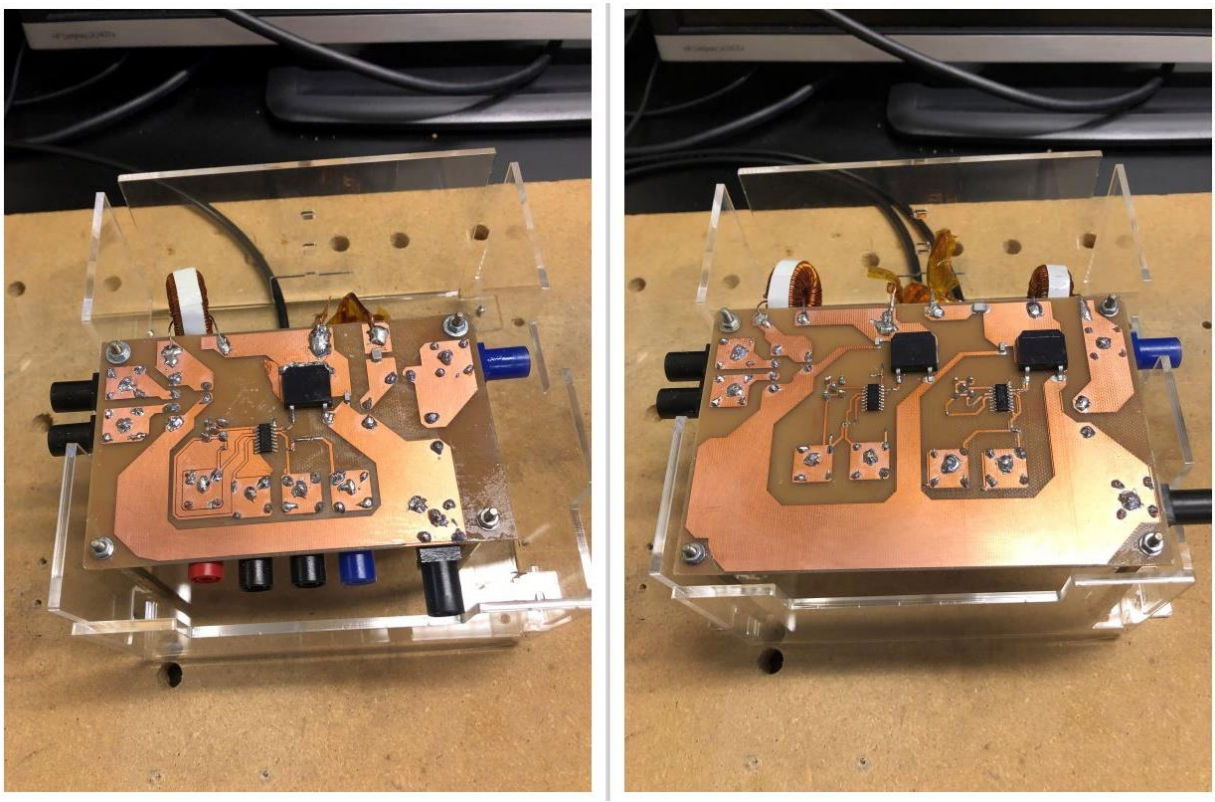

Figure 27. The first and second suggested converter designed at UiT campus Narvik.

The PCBs are designed to be small while keeping a minimum distance between traces and components. Saturn PCB design are used to ensure minimum required distance for the expected voltage, and the resonant circuit is kept to a minimum with the shunt capacitor close to the transistors to minimize ringing [3]. Appendix C shows mechanical footprint of the PCBs.

Current sensor

To measure resonant current for each of the circuit without a current probe, the plan was to design and make a current sensor PCB that was added in the resonant loop. The component needed for this PCB was not delivered in time. therefore, it was not possible to measure the current through the experimental test. Figure 40 shows the designed current sensor and mechanical footprint is found in Appendix C.

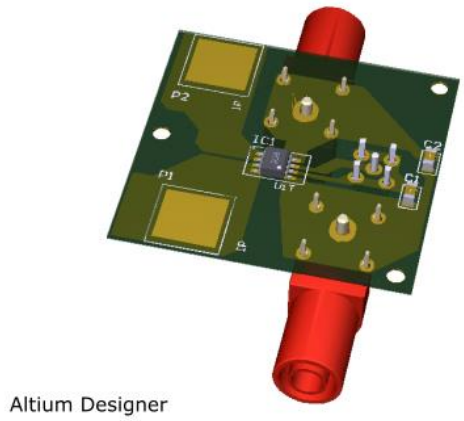

Figure 28. Current measuring PCB

6 Simulated results

Simulations of converters with component values listed in table 8.

Table 8. Component used in simulation of the suggested converter.

Passive components	First suggested converter	Second suggested converter
Input capacitor, C_{IN}	1 μF	1 μF
Load resistance, R_L	401 Ω	401 Ω
Resonant inductor, L_r	86,3 μH	86,3 μH
Shunt capacitor, C_{S1}	220 pF	270 pF
Resonant capacitor, C_r	470 pF	470 pF
Choke inductor, L_{IN}	1 mH	1 mH
Filter capacitor, C_F	560 μF	560 μF

Input capacitor is chosen to be 1 μF and according to [32] used to absorb reverse current from the inverter, suppress EMI and eliminate AC components at the output of the bridge. Further, the resistance is calculated by equation (4,10) and reflected to the load resistance by (4,19).

Shunt capacitor differs from its calculated due to parasitic capacitance in the MOSFET. The parasitic effect of the MOSFET is changed by the frequency and voltage and appear though these circuits higher than given in datasheet. Changing shunt capacitor affects the voltage stress and hence, the ZVS capability of the converter. This is explained in chapter 6.2 and shown in figure 32 and figure 33.

6.1 The first suggested converter

Figure 29 shows the grid voltage, output voltage, grid current and input inductor current. Alignment of the currents shows PFC capability of the converter. The input inductor current is plotted with the grid current to show that the absolute value of the frequency is equal, stated in (4,1) and (4,2).

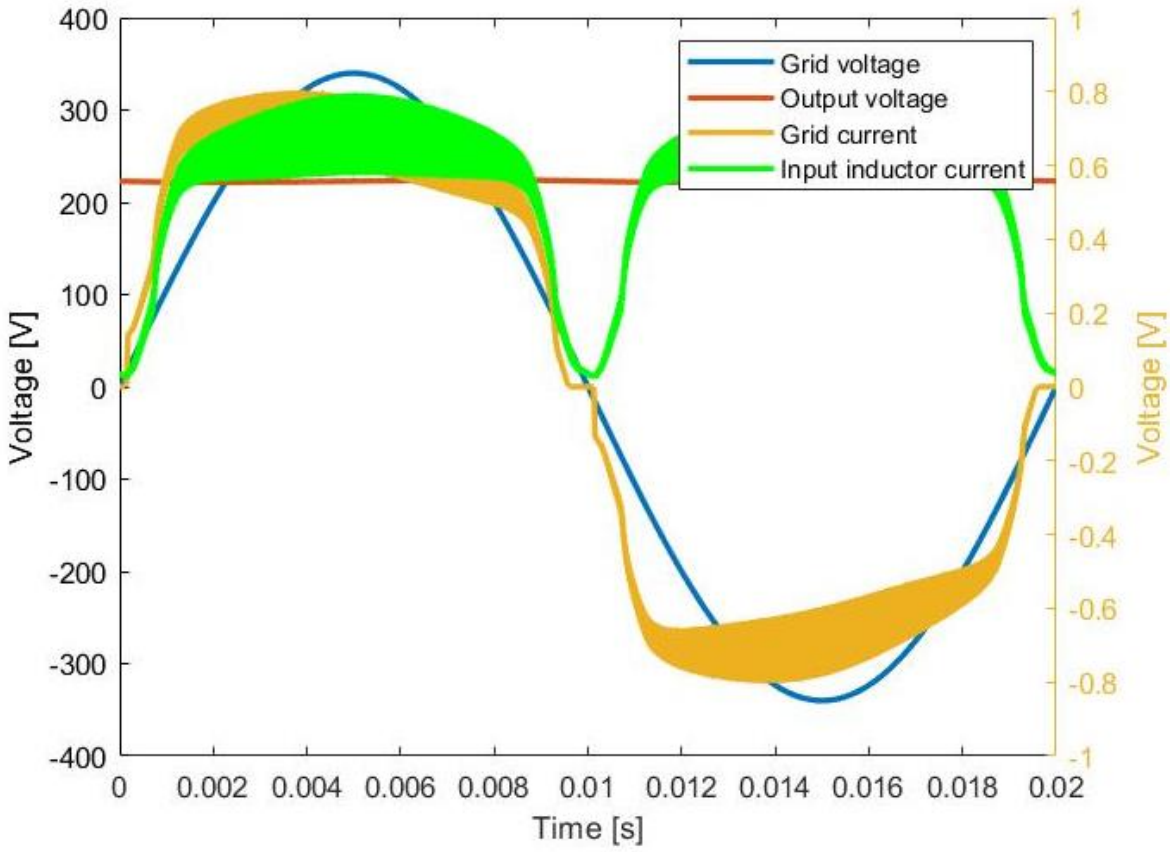

Figure 29. Simulation of grid voltage, output voltage, grid current and input inductor current of the first converter

Figure 29 shows an output voltage of 223 V and a grid current of 0.59 A. This gives an output power of 124 W and a input power of 137 W. Figure 30 shows the drain-to-source voltage, gate voltage, and drain-to-source current. The MOSFET achieves soft-switching at both turn on and turn off. This means that the switching loss is eliminated. However, the period from reaching zero voltage switching and until the gate voltage turns on, shows that the converter is switching in suboptimal condition. At this condition, the voltage turns negative for a short period where the body diode is conducting. The negative drain-to-source current passing the body diode generates body-diode loss.

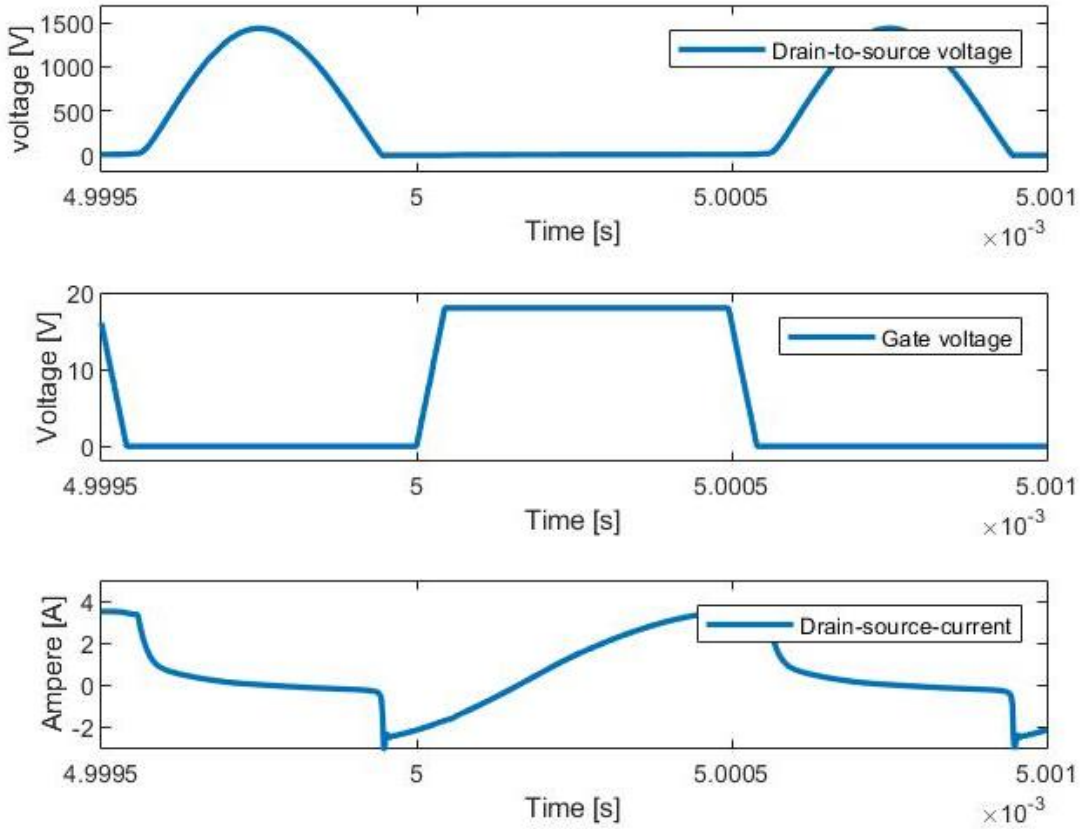

Figure 30. Simulation of drain-to-source voltage, gate voltage and drain-to-source current for the first converter.

Figure 31 shows the transistor drain-to-source voltage and current across the line-cycle. As menioned chapter 3.2, the average value of the transistor drain-to-source voltage equeals the RMS vaule of the applied grid voltage. Through simulation, the average value is close, and not equal to the grid voltage. The difference between the average value of drain-to-source voltage and the input RMS value is affected by the shunt capacitor.

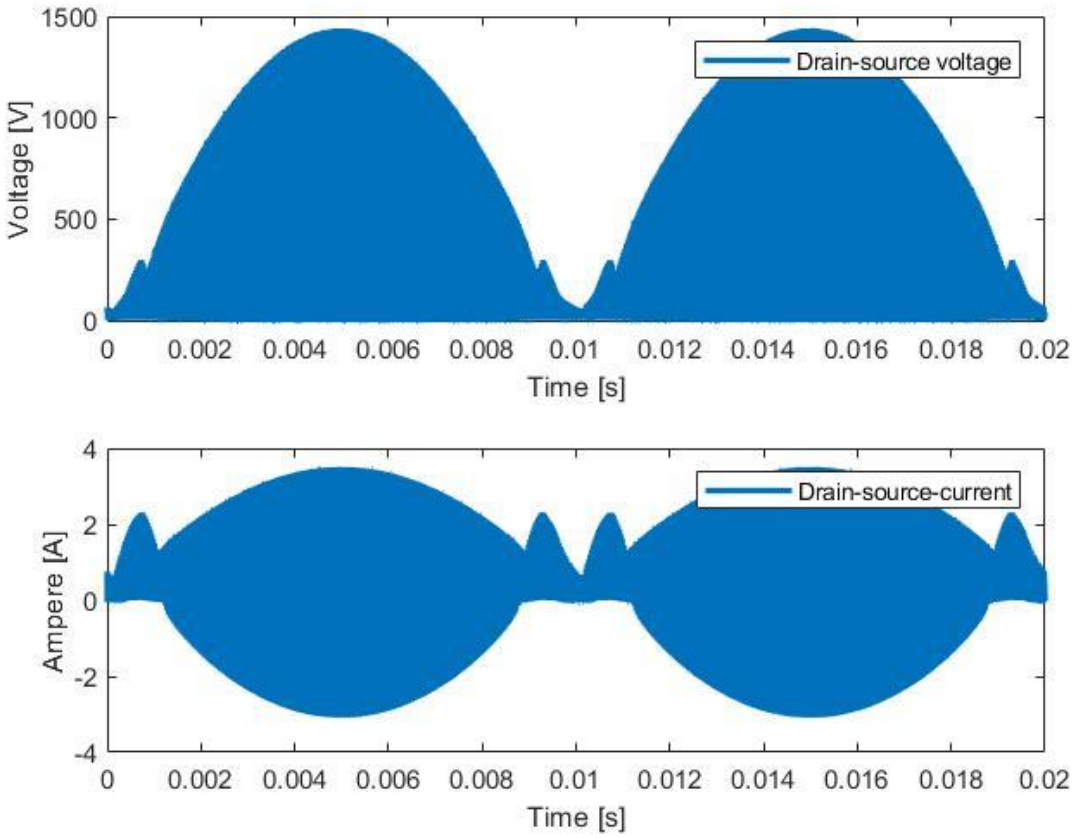

Figure 31. Simulated drain-to-source voltage and current of the first converter.

The shunt capacitor is smaller than the calculated value due to parasitic capacitance in the MOSFET, as the parasitic capacitance and the shunt capacitance are added into what the converter see as the shunt capacitance. The parasitic effekt is non-linear reversely proportional to applied voltage, where it is large when the voltage across is small. Similary, it is small when the drain-to-source voltage is high. With a small shunt capacitor, the ZVS condition holds for a larger period when the applied voltage across the transistor is low, shown in figure 31. This happes as the drain-to-source voltage-curve reaches zero faster during discharging. However, the peak value of the drain-to-source voltage increases and will be higher than given in equatuon (4,7) and (4,8).

Increasing the shunt capacitor has opposite effect, hence, it reduced the voltage stress but the ZVS condition does not hold. Figure 32 shows the difference in simuation when the shunt capacitor is 270 pF compared to 220 pF, where 220 pF is used in the first suggested converter and 270 pF is used in the second suggested converter.

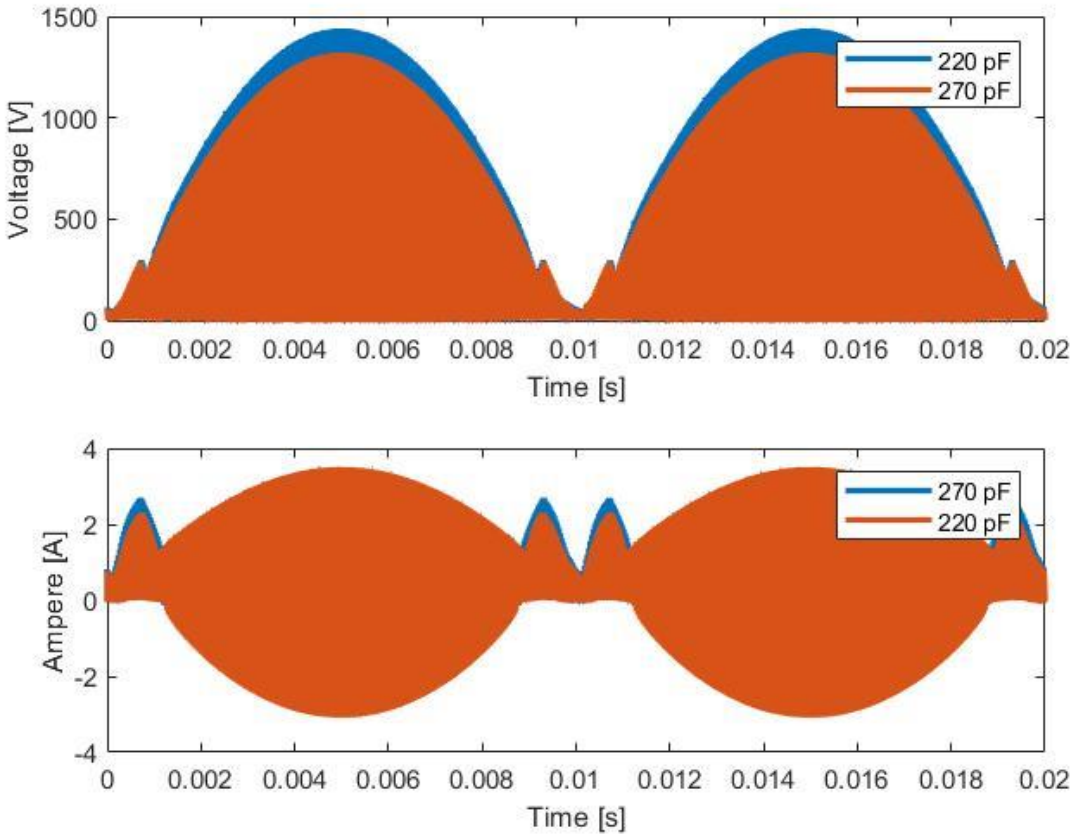

Figure 32. Difference in drain-to-source voltage and current when changing the shunt capacitor from 220pF to 270pF for the first suggested converter.

The figure 32 shows the voltage and current stress across one cycle of 50Hz for both 220 pF and 270 pF. Note that the upper figure shows the proposed value, 220 pF, in blue, while the lower figure show this value in orange. This is done to highlight the stress with both alternative. Figure 33 shows the the voltage stress to highlight the ZVS condition with both sizes of the shunt capacitor. As mentioned above, the figure shows that the ZVS condition holds for a larger periode of time when chosing a lower shunt capacitor.

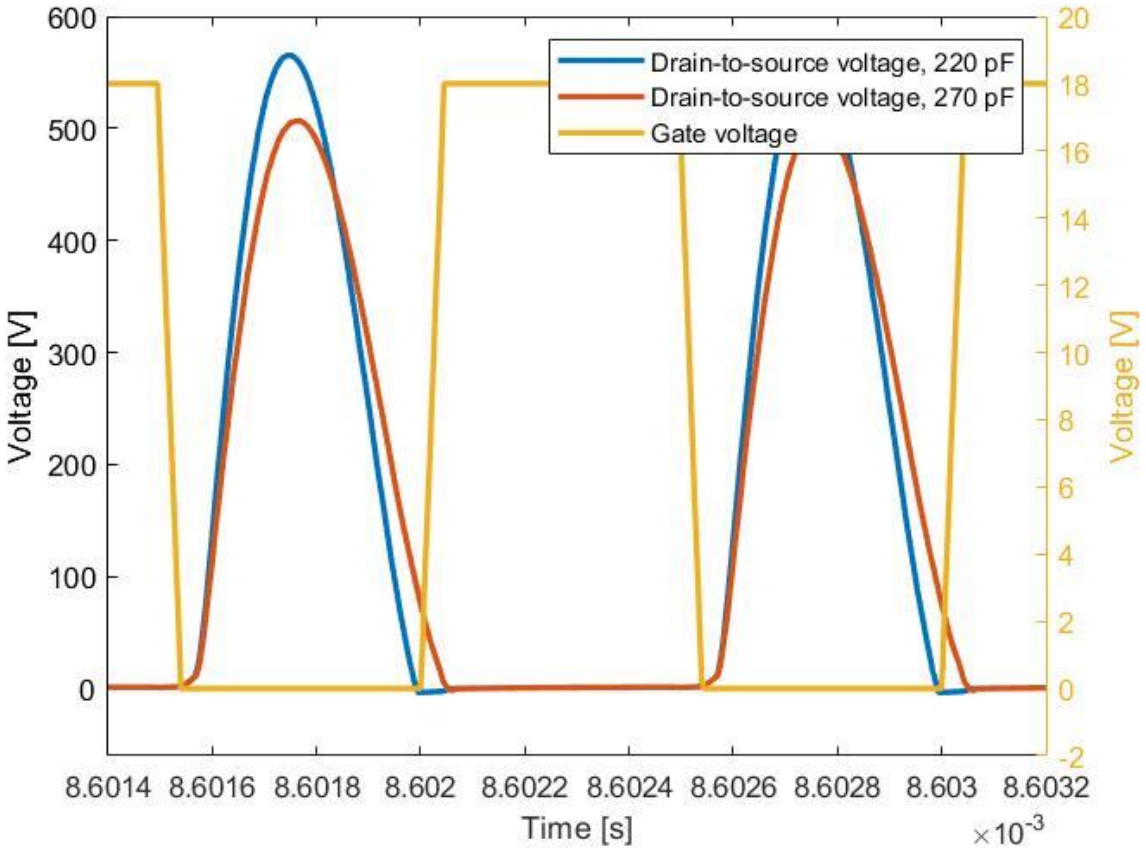

Figure 33. ZVS capability for 220 pF and 270 pF at the first suggested converter.

Further, Figure 34 shows the drain-to-source voltage and current across two switching cycles during the current spikes. At these periods, the switch turns off at zero drain-to-source voltage, but not on.

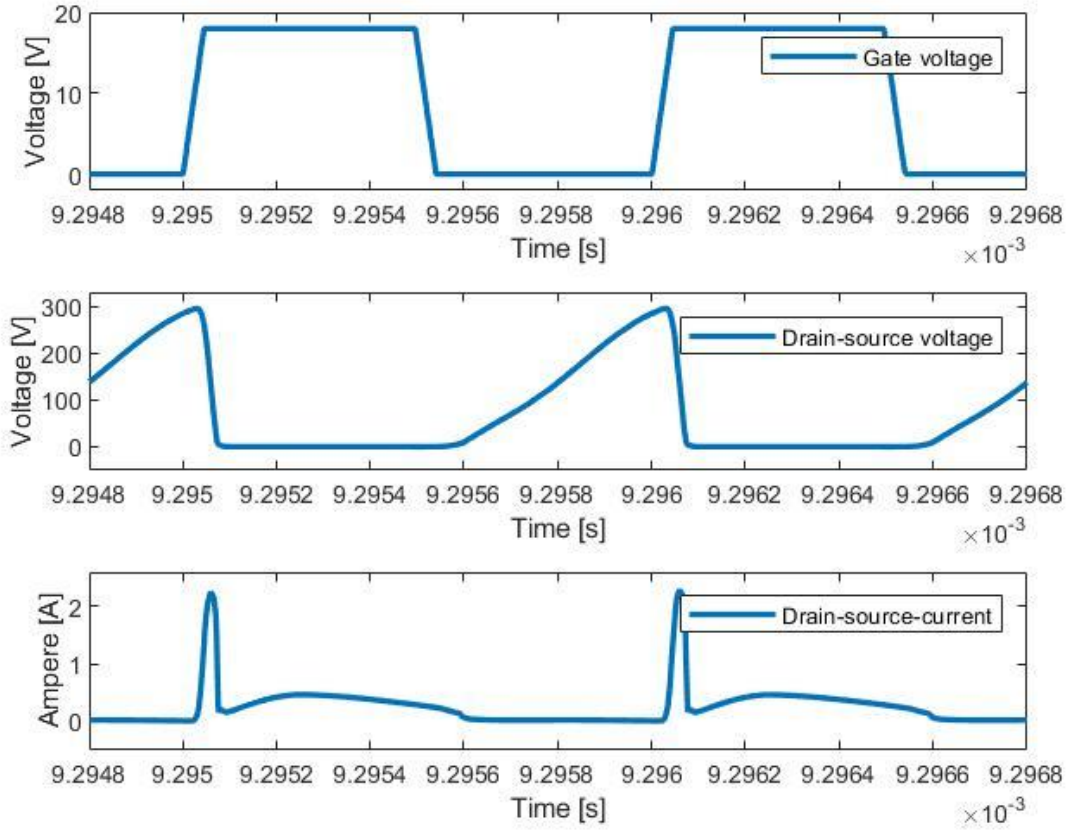

Figure 34. Simulated result of gate voltage and drain-to-source voltage and current during low voltage across the transistor for the first suggested converter.

6.2 The second suggested converter

Figure 35 shows simulations of voltage and current for the second proposed converter. Aligned grid voltage and current confirms PFC capabilities of the converter.

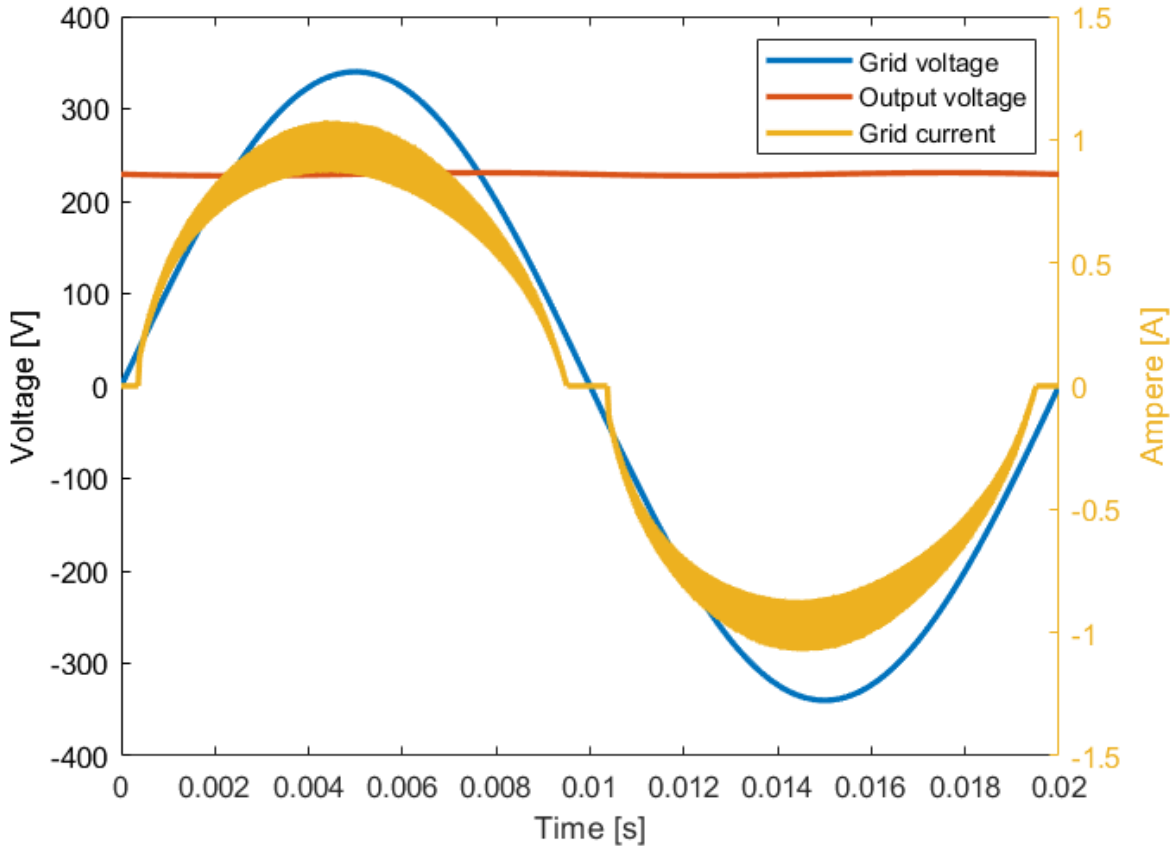

Figure 35. Simulated grid voltage, output voltage and grid current for suggested converter 2.

Figure 35 shows an output voltage of 229 V and a gird current of 0.73 A. Resulting in an output power of 131 W and an input power of 173 W. Figure 36 shows the grid current, input inductor current and output inductor current across one line cycle of 50 Hz. Comparison the inductor current and grid current shows that the absolute value of the frequency is equal.

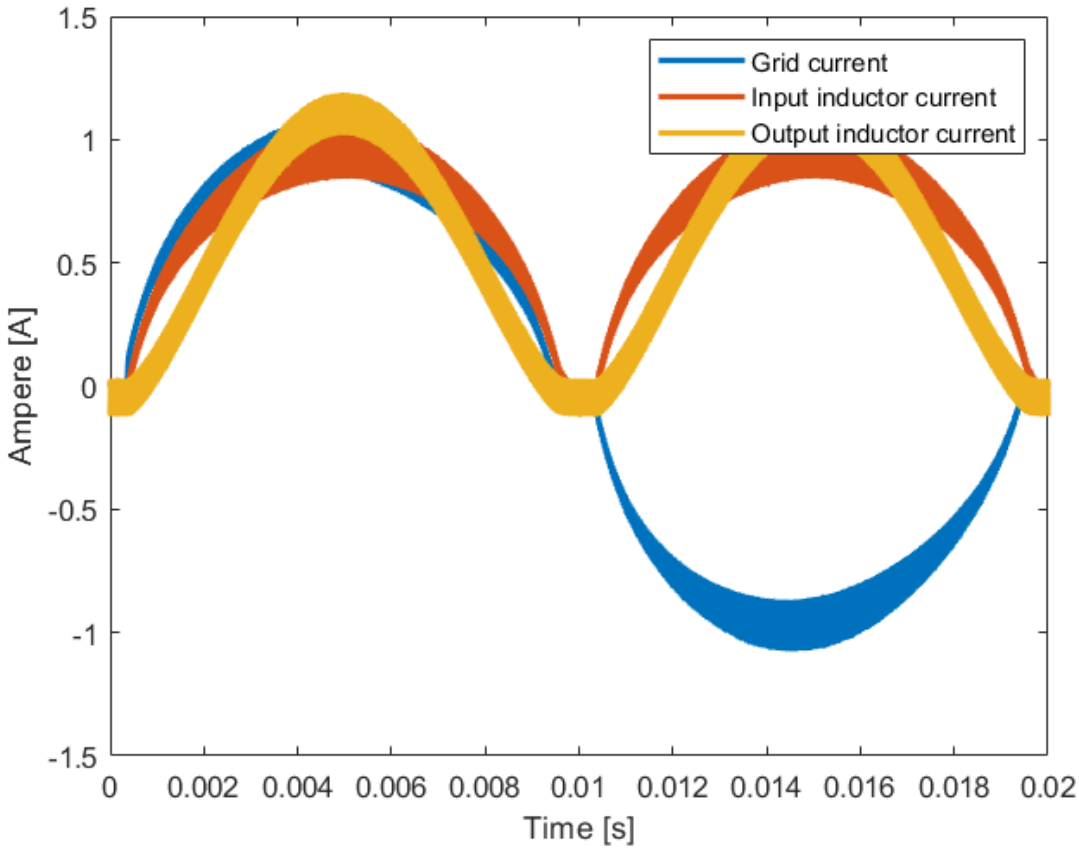

Figure 36. Simulation of grid current, input inductor current and output inductor current for the second suggested converter.

Figure 37 shows the drain-to-source voltage, gate voltage, and drain-to-source current of both transistors, where ZVS is verified during switching on and off. This means that the switching loss are eliminated. However, a negative drain-source voltage which indicates that the converter operates in suboptimal condition, confirmed by the negative drain-source current. This current passes through the body diode and generates body diode loss to the converter.

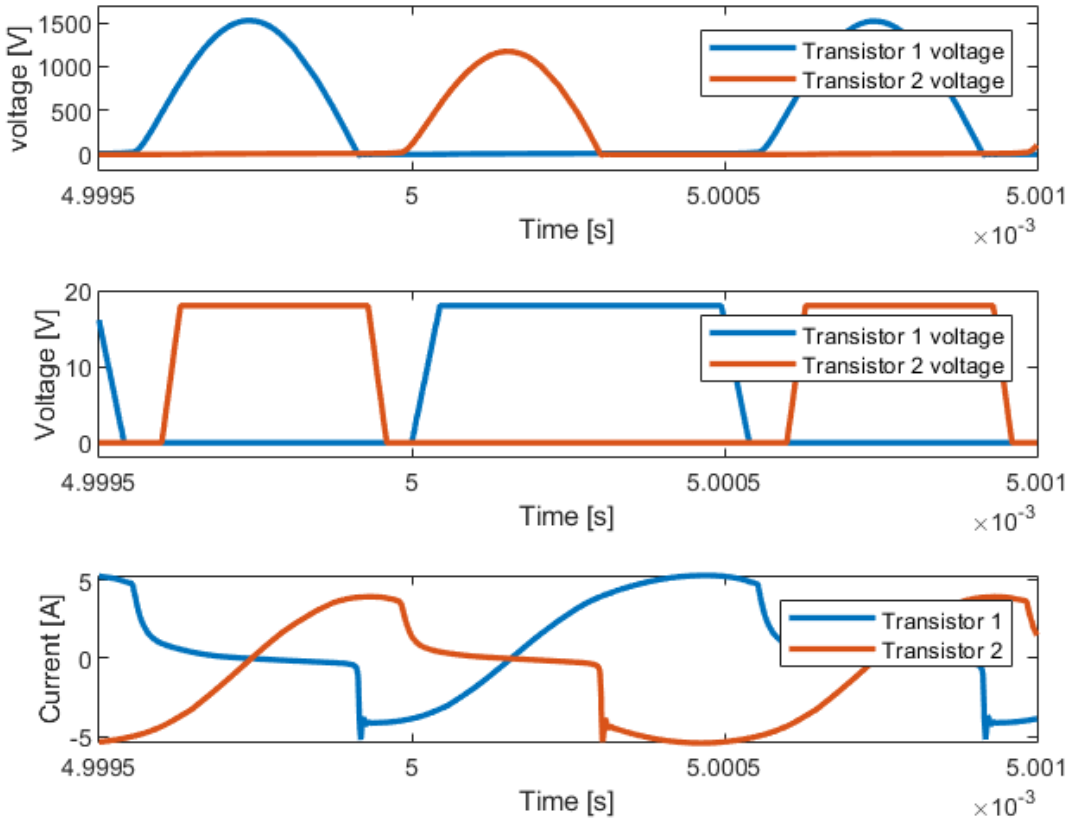

Figure 37. Simulated switching-frequency-cycle result of the transistor gate voltage, drain-to-source voltage and drain-to-source current for the second suggested converter.

Figure 38 shows the transistor drain-to-source voltage and current across the line cycle. The average value of the voltage across transistor S_1 is close to, and not equal to the RMS value of the connected grid voltage. However, the average value of the voltage across transistor S_2 equals the average value of the output voltage. Note that in the upper plotting of figure 36, the voltage across transistor 2 is plottet first to highlight the voltage across transistor 1.

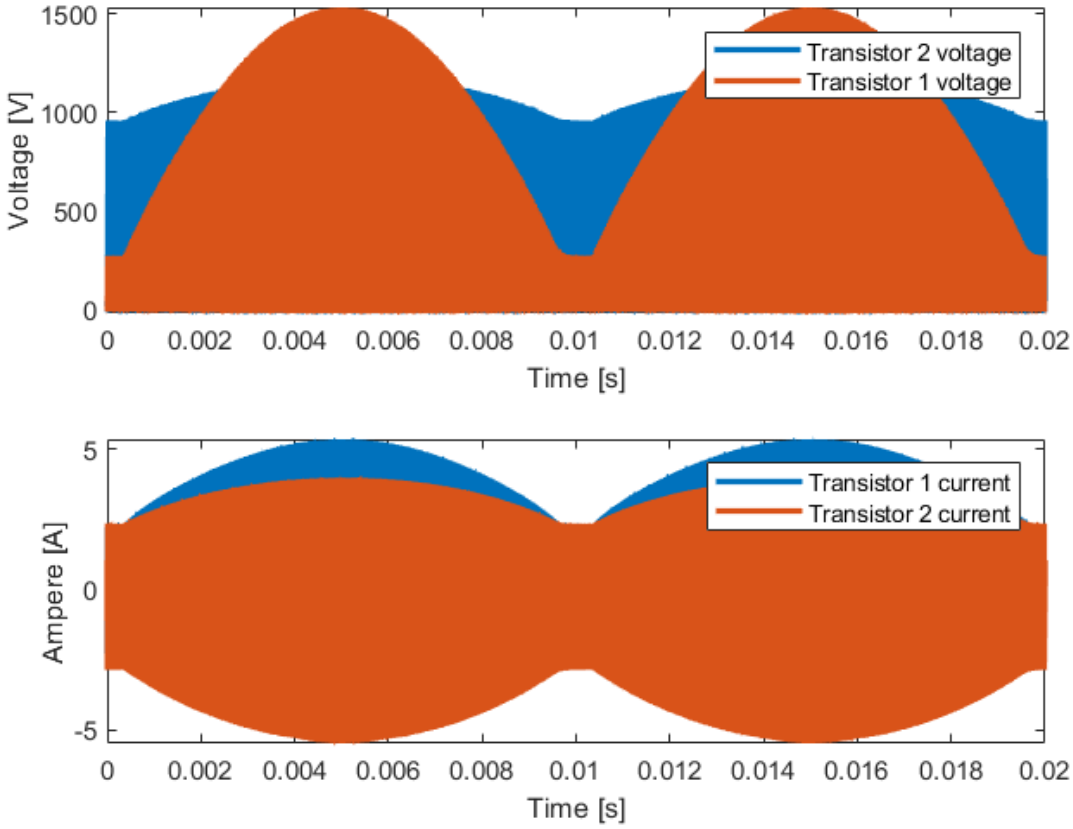

Figure 38. Simulation of drain-to-source voltage and current across one periode of 50 Hz for the second suggested converter.

Comparing figure 39 against figure 31 shows that this converter avoids the prone voltage and current spikes that occurred during the low-voltage period. Figure 37 shows ZVS capability during the low-voltage period.

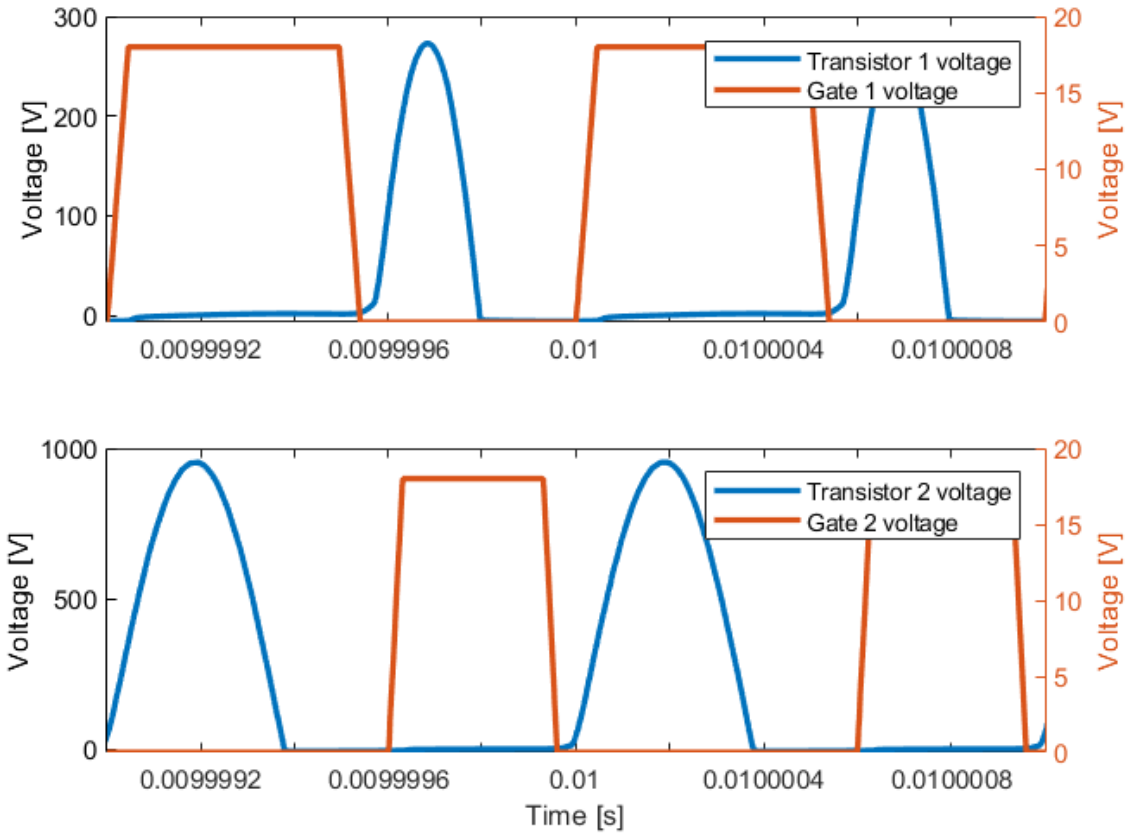

Figure 39. Simulation of ZVS across two switching-cycles for second suggested converter during low drain-to-source voltage.

For a comparison, figure 40 shows the voltage across each transistor with a shunt capacitor of 220 pF and 270 pF. The figure shows that the maximum voltage stress across transistor 1 was 1650 V with a shunt capacitor of 220 pF and 1525 V with a shunt capacitor of 270 pF. As the chosen transistors have a limitation of drain-to-source voltage at 1700 V, the shunt capacitor was set to be 270 pF.

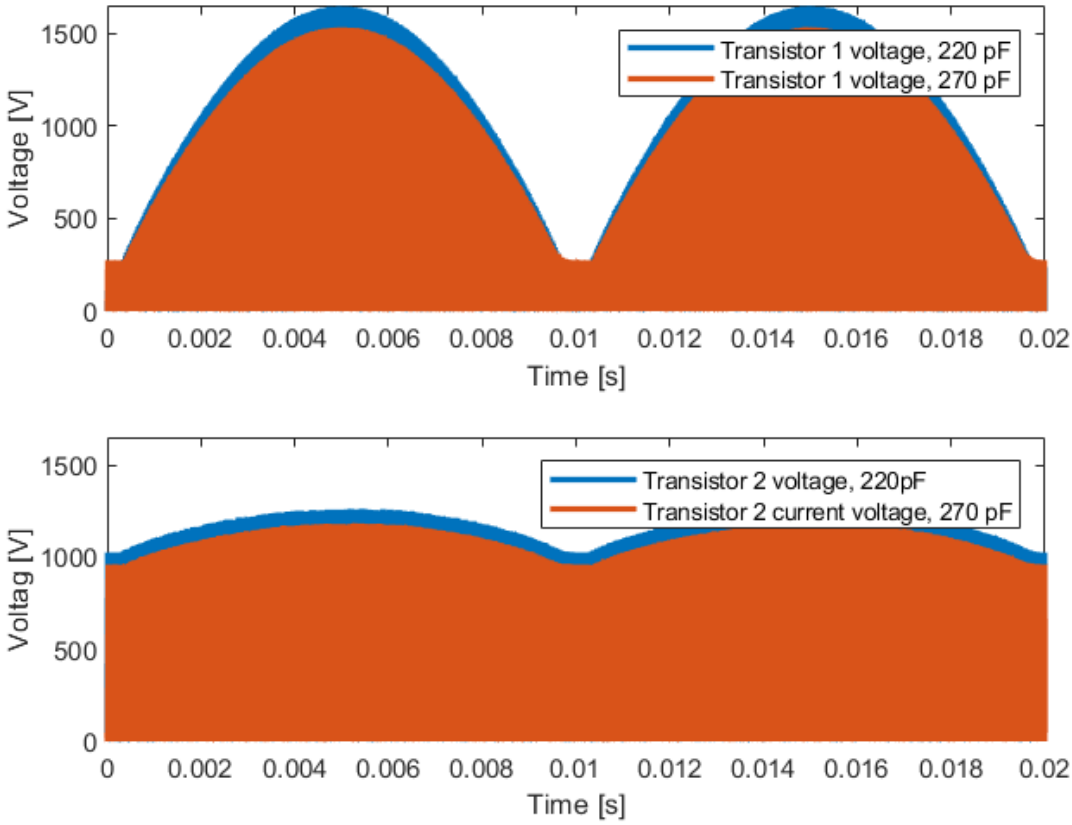

Figure 40. Simulation of a comparison between drain-to-source voltage and current across line-cycle with 220 pF and 270 pF shunt capacitor for the second suggested converter.

6.3 Simulation summarize

Simulation of the converters shows PFC capability at high frequency and ZVS at the converter values. However, the first converter experience switching on at non-zero values when low drain-to-source voltage across the transistor.

The converters were design to step down the voltage and to work for 300 W. Simulation showed that the first suggested converter gave 223 V at 124 W output, and the second suggested converter gave 229 V at 131 W output. This is a result of the converter gain according to (4,17) and (4,25), where the designed power is set as input power.

7 Experimental result

Converters were tested to verify the design. Component values and switching frequency is listed in table 9, and equipment used through testing is shown in table 10. Figure 41 shows the test bench with the equipment used.

Table 9. Component values and switching frequency used through testing.

Component	First suggested converter	Second suggested converter
Input capacitor, C_{IN}	1 μF	1 μF
Load resistance, R_L	401 Ω	401 Ω
Resonant inductor, L_r	86.4 μH	86.4 μH
Shunt capacitor, C_S	220 pF	270 pF
Resonant capacitor, C_r	580 pF	470 pF
Inductor, L_{IN} and L_{OUT}	1 mH	1 mH
Filter capacitor, C_F	560 μF	560 μF
Frequencies		
Frequency	1 MHz	1 MHz

Testing is done with a higher resonant capacitor in the first converter to offset the parasitic capacitance of diodes in the rectifier. These diodes appear in series with the resonant circuit and makes the parasitic capacitance appear in series with the resonance capacitor. This is further elaborated in Trouble shooting in chapter 7.3.

Table 10. Equipment used through testing of the converters.

Description	Equipment
Adjustable voltage meter	California Instrument 2253iX
Signa generator	Hewlett Packard 33120A
Voltage regulator	GW Laboratory DC Power supply GPS-3030
Voltage regulator	EA Power supply EA-PS 2042-20B
Impedance tester	Hewlett Packard 4285A
Load resistance	ASEA Education variable resistor 630 W
dSPACE	dSPACE CLP1104Voltage converter
Oscilloscope	Agilent Technologies DSO-X 2004A
Power analyser	Keysight IntergraVision PA2203A
Multimeter	Fluke 89 IV True RMS multimeter

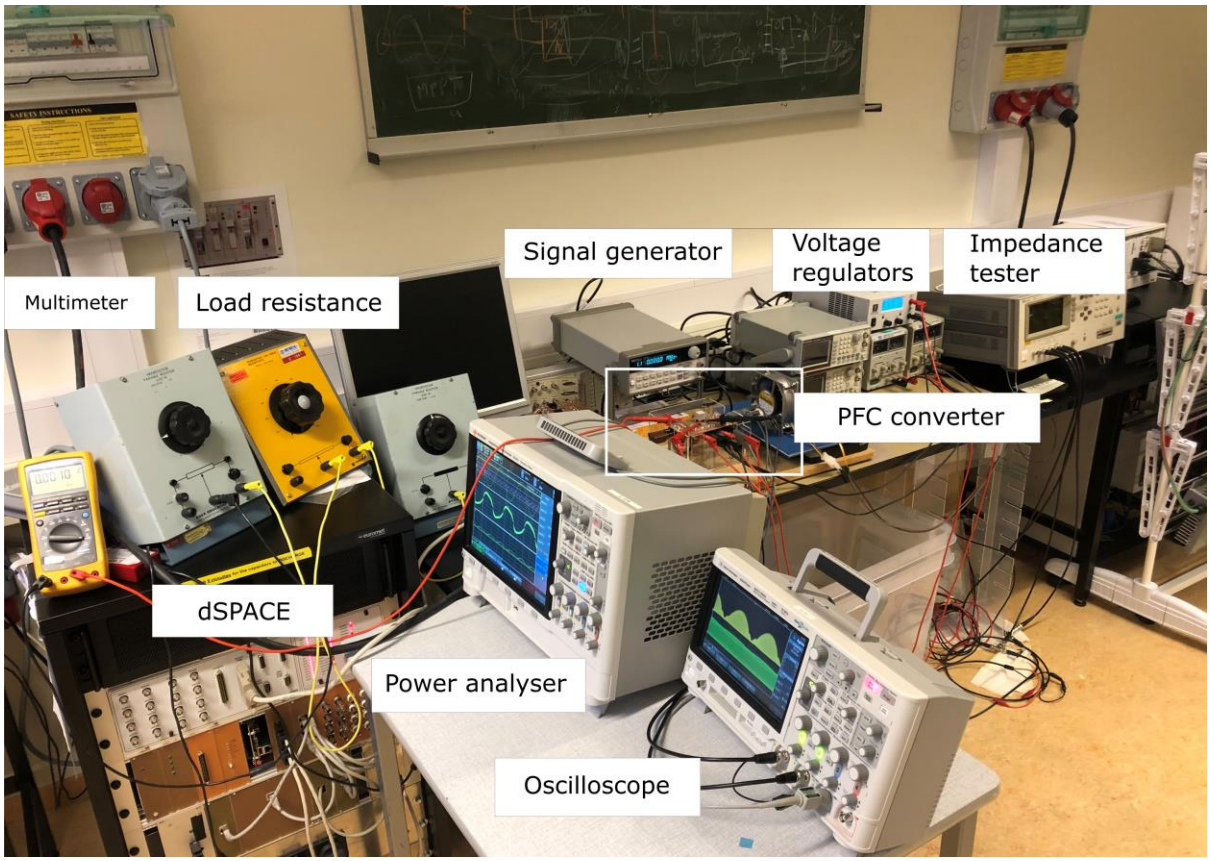

Figure 41. Equipment used through testing of converters.

7.1 The first suggested converter

The first converter is tested at voltages from 85 V - 240 V/50 Hz and 120 V/ 60 Hz, where 240 V/ 50 Hz and 120 V/ 60 Hz is evaluated.

240 Voltage at 50 Hz

Figure 42 shows the grid voltage, grid current and the output voltage of the converter. The figure shows an output average voltage of 80.8 V and a rms value of the grid current of 0.23 A. Alignment of current and voltage shows PFC capabilities.

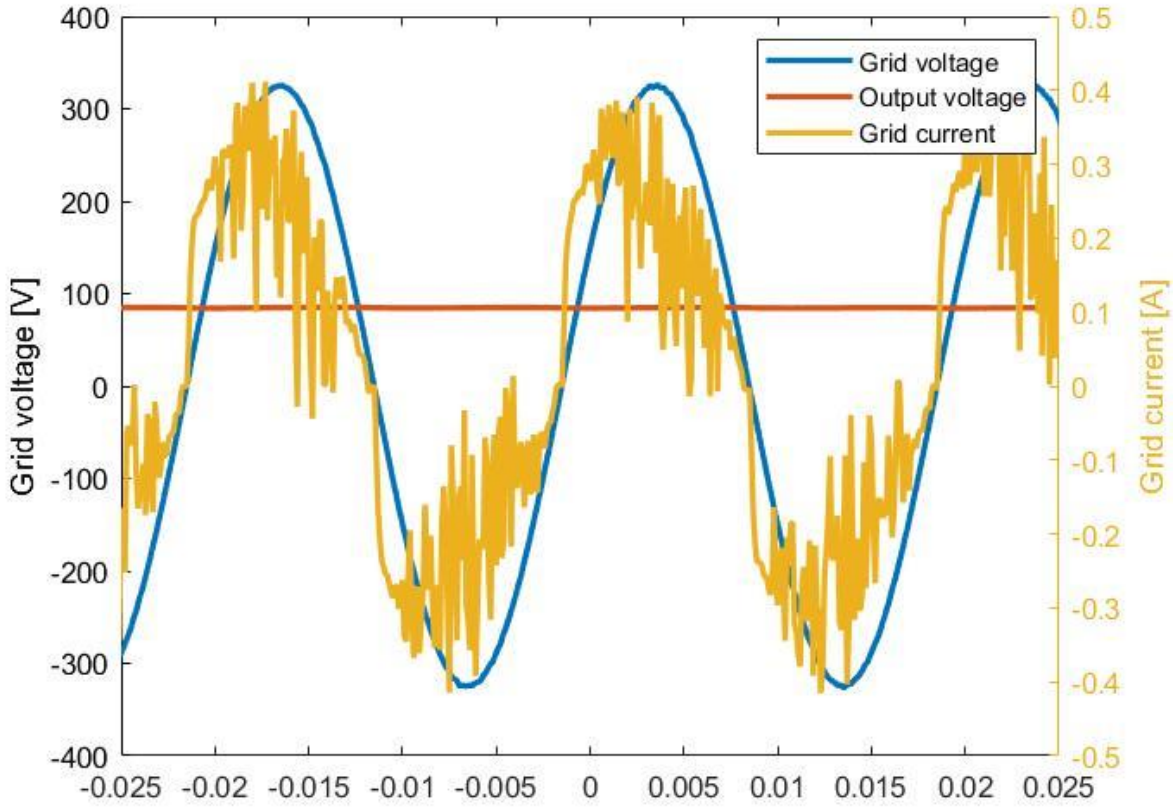

Figure 42. Grid voltage, output voltage and current across line cycle testing at 240 V/ 50 Hz for the first converter.

Figure 43 shows harmonic distortion of the current, harmonic limits for a Class C equipment and input and output power. The harmonic content is measured at the grid current from the fundamental frequency and up to the 40^{th} harmonics and plotted with the limits of Class C equipment according to IEC 61000-3-2. THD and power factor PF are 25.95 % and 0.93, where the fundamental frequency is 50 Hz. The efficiency of the converter is measured to 40.22 %, with an average input power of 44.2 W and an average output of 17.8 W.

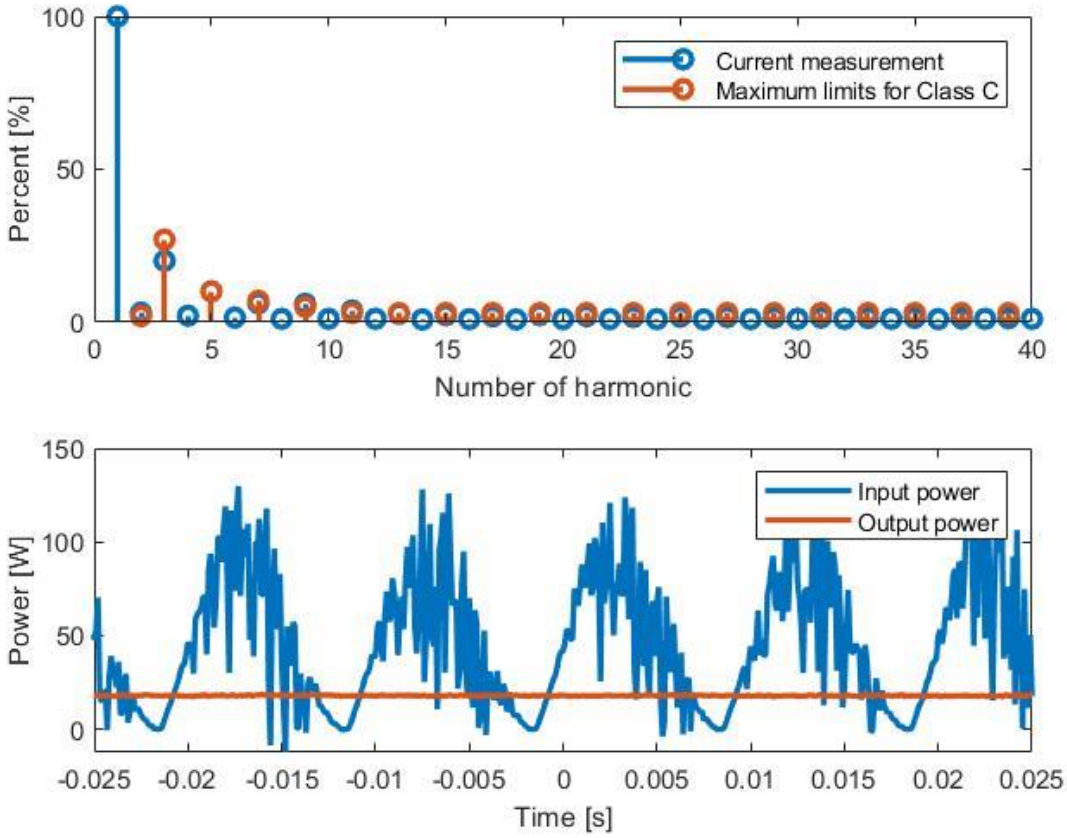

Figure 43. Harmonic content, maximum limits for Class C equipment according to IEC 61000-3-2 and power tested for the first converter at 240 V/ 50 Hz.

Figure 44 shows the drain-to-source voltage across the transistor and transistor gate voltage over a switching cycle, and the drain-to-source voltage across a half line cycle of 50Hz. The converter operates in suboptimal condition with body diode condition and switching off at non-zero value. Suboptimal operation is shown by the slope of the switch voltage, and that the switch voltage drops below zero. Switching off at non-zero value affects the efficiency.

During the periods with low voltage across, the same behaviour as seen in figure 31 occur. However, this effect is not as prone with the chosen parameter and not visible on the figure because of a low number of plots from the oscilloscope. The peak value of the drain-to-source voltage across the line cycle shows a voltage stress lower than the simulated and calculated values.

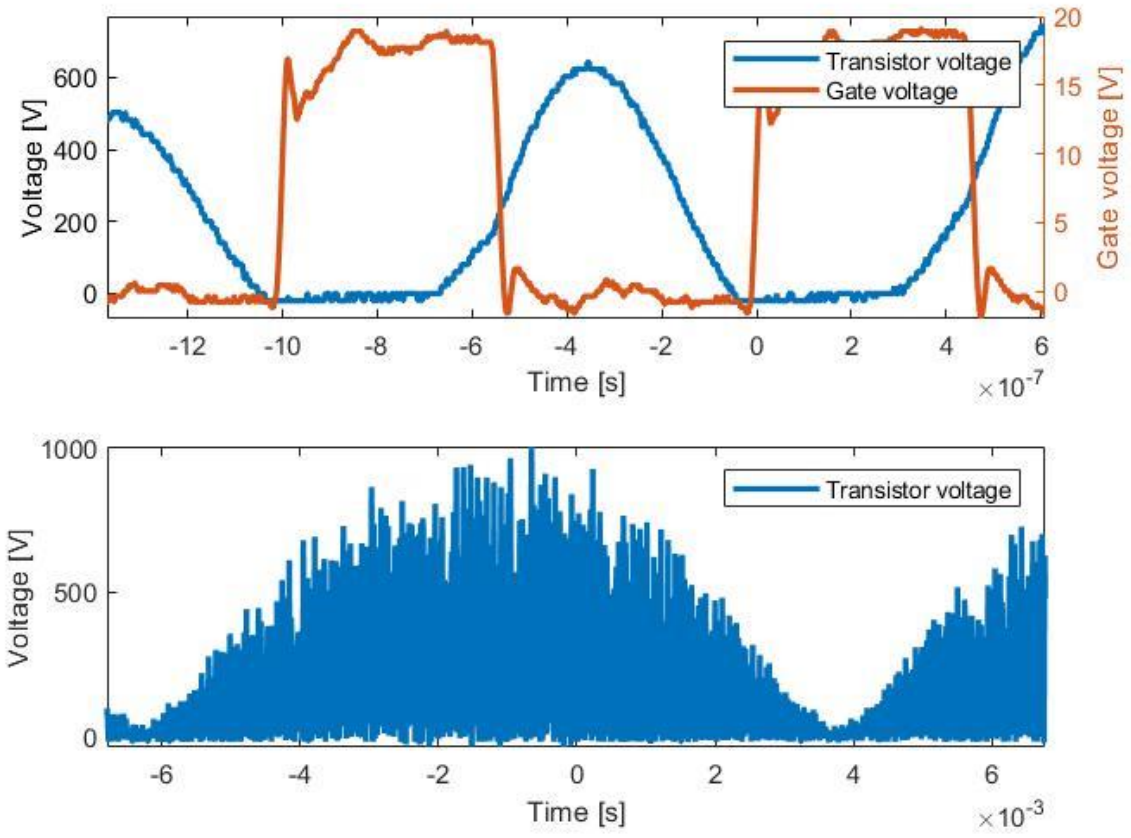

Figure 44. Drain-to-source and gate voltage across switching cycles and drain-to-source voltage across line cycle for the first converter.

Figure 45 shows the temperature of the transistor during testing. High temperature while low performance of the converter reveals switching loss and diode conduction loss. Debugging has been carried out and is elaborated in chapter 7.3.

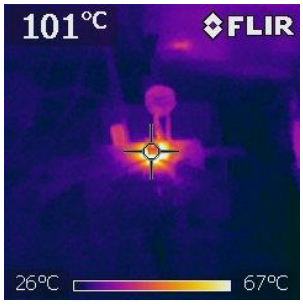

Figure 45. Temperature during testing of the first suggested converter at 240 V/ 50Hz.

120 Voltage at 60 Hz

Figure 46 shows grid voltage, grid current and the output voltage of the converter. Alignment of voltage and current shows the same behaviour as for the 240 V/ 50 Hz. The average output voltage is 64.75 V and RMS value of the grid current is 0.16 A

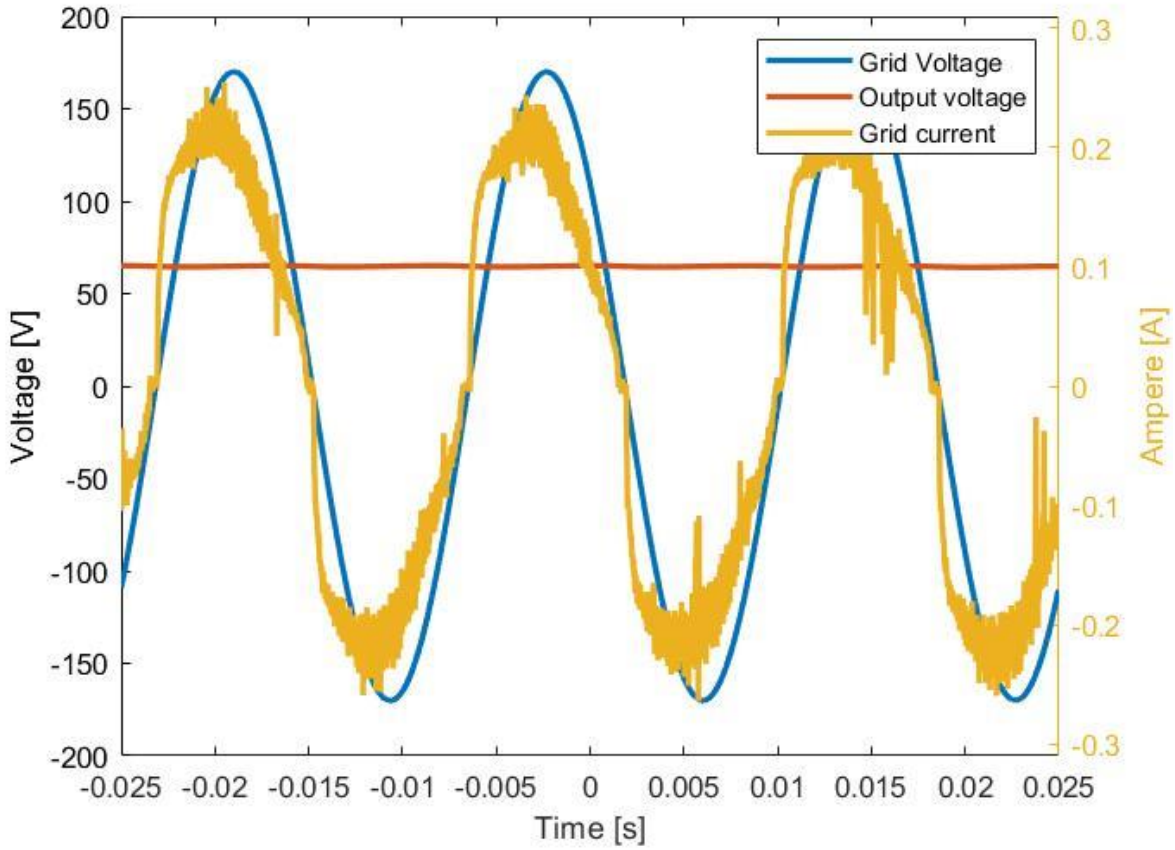

Figure 46. Grid voltage, output voltage and grid current for the first suggested converter at 120 V/ 60 Hz.

Figure 47 shows the drain-to-source and gate voltage across switching cycle, and the input and output power of the converter across line cycles. The figure shows suboptimum operation and switching off at non-zero voltage, the same behaviour as for 240 V/ 50 Hz in figure 44.

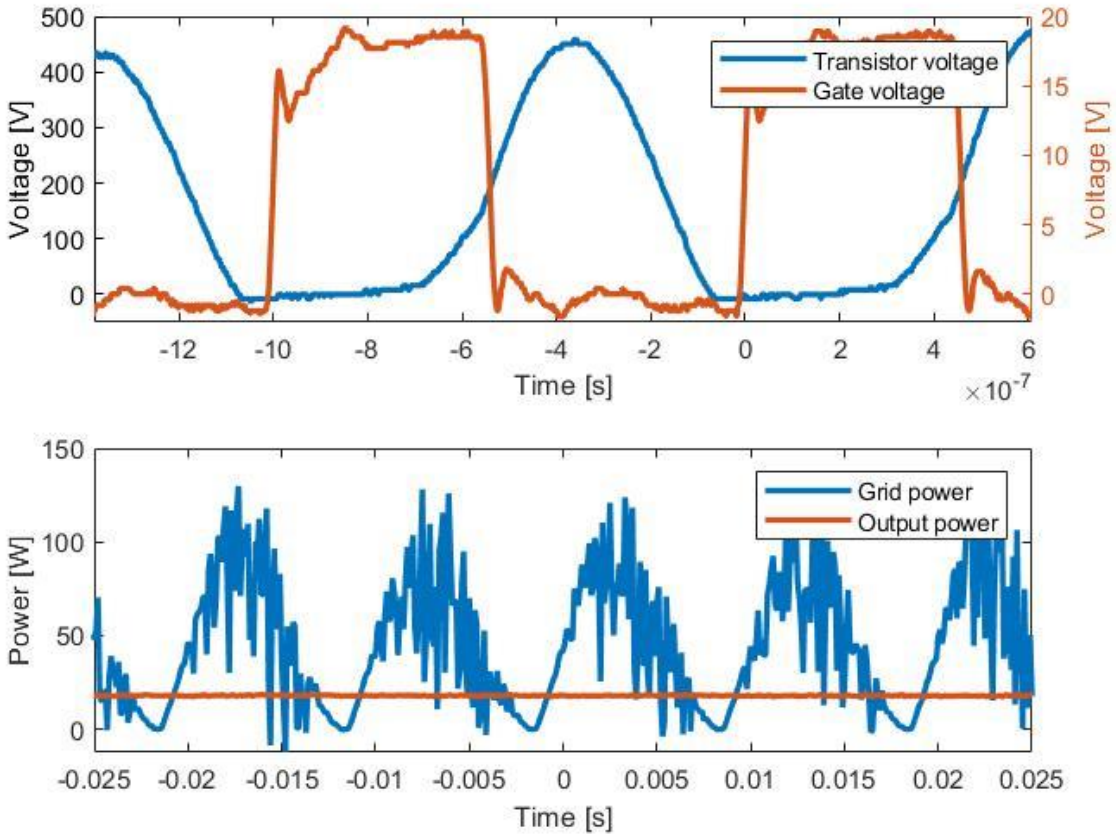

Figure 47. Drain-to-source and gate voltage across switching cycle and power across line cycle for the first suggested converter at 120 V/ 60 Hz

Figure 48 shows the temperature during testing for the applied voltage. High temperature with low power output confirms switching losses and diode conduction losses.

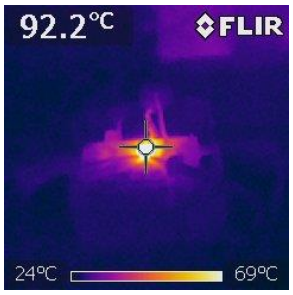

Figure 48. Temperature measured on the transistor during testing of the first suggested converter at 120 V/ 60 Hz.

7.2 The second suggested converter

The second proposed converter is tested for 85 V/ 50 Hz and 120 V/ 60 Hz, where 120 V/ 60 Hz is shown. It is not tested for higher voltage due to performance. Debugging was conducted at for the first converter and is elaborated in trouble shooting in chapter 7.3.

120 Voltage at 60 Hz

Figure 49 shows grid voltage, grid current and the output voltage of the second converter. The average output voltage of the converter is 98.6 V, and the RMS value of the gird current is 0.55 A.

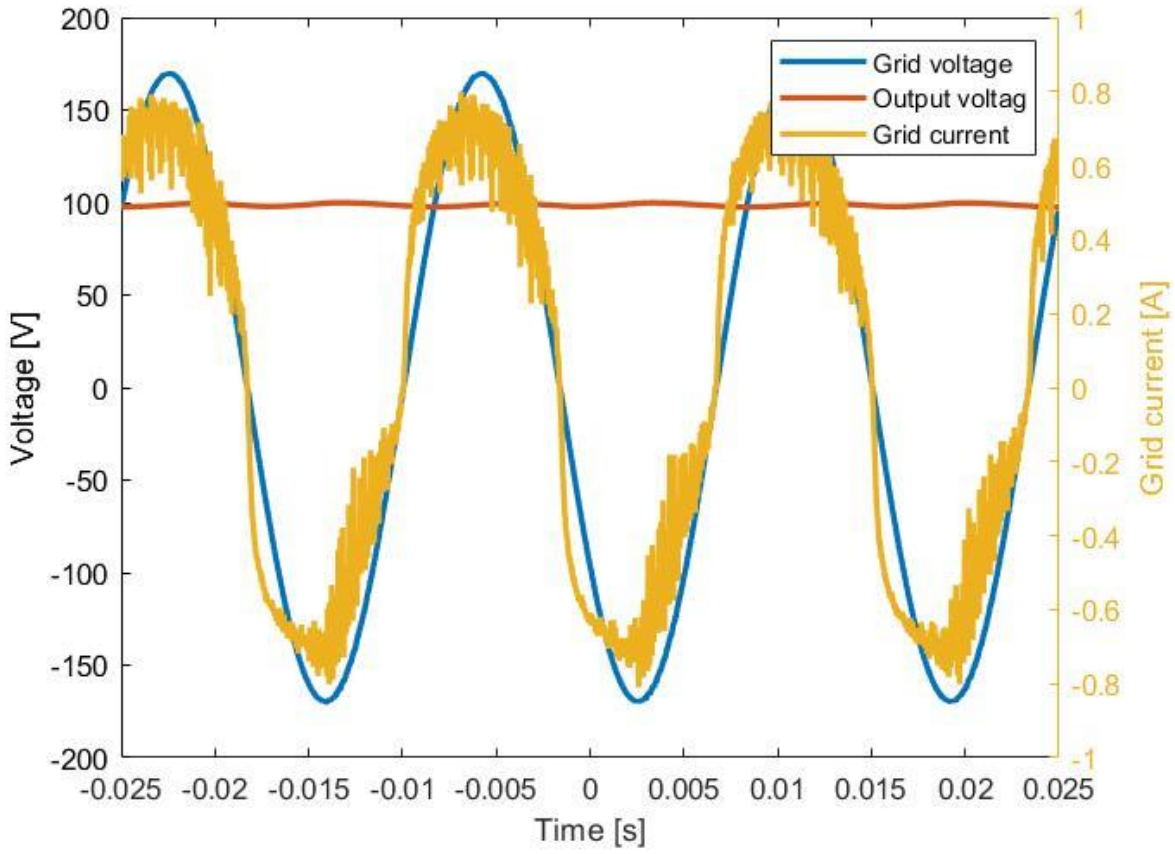

Figure 49. Grid voltage, output voltage and grid current for the second suggested converter at 120 V/ 60 Hz.

Figure 50 shows the harmonic content plotted with the maximum limits according to IEC 61000-3-2 and the power across line cycles. IEC 61000-3-2 account for application meant for 240V. The Total harmonic distortion, THD, is 17.96 % with the fundamental frequency at 60 Hz. The efficiency of the converter 38.0 %, with an average input power of 63.6 W and an average output of 24.1 W.

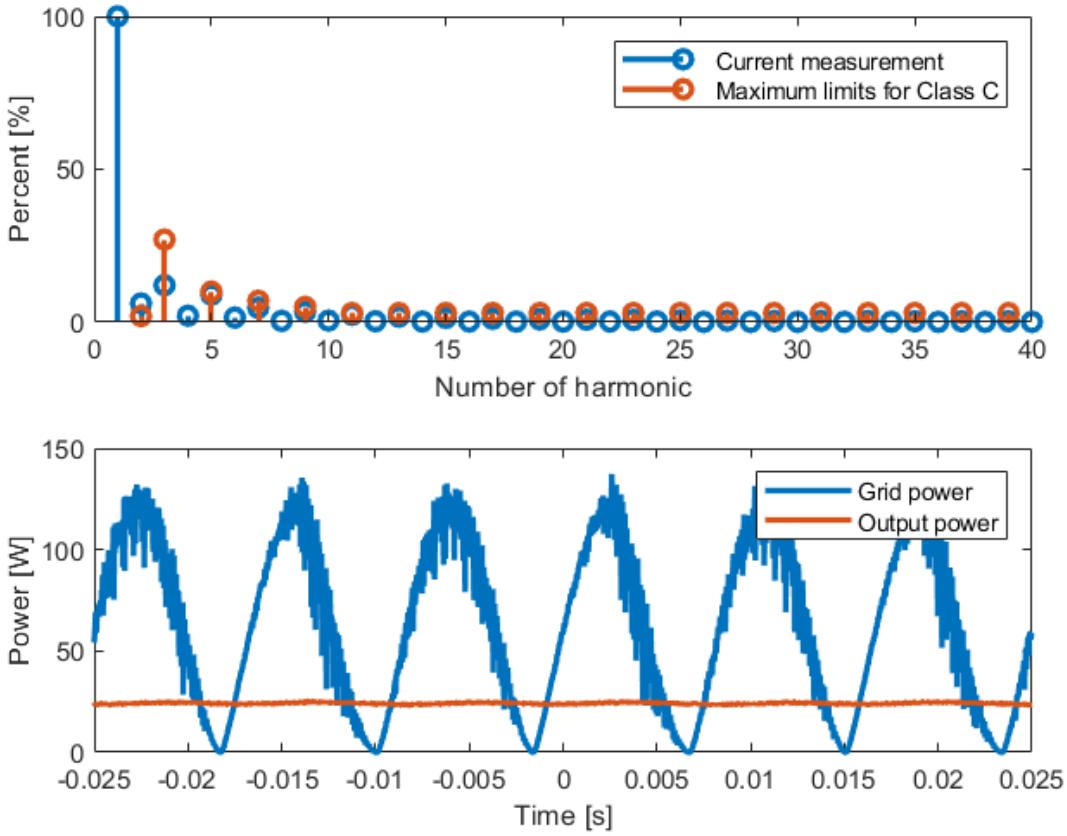

Figure 50. Harmonic content, maximum limits for Class C equipment according to IEC 61000-3-2 and power tested for the second converter at 120 V/ 60 Hz.

Figure 51 shows the drain-to-source voltage across transistor 1 and the gate voltage of transistor 1 and transistor 2. The duty cycle is 0.45 for transistor 1 and 0.3 on transistor 2. The figure shows suboptimal operation with switching off transistor 1 at non-zero value.

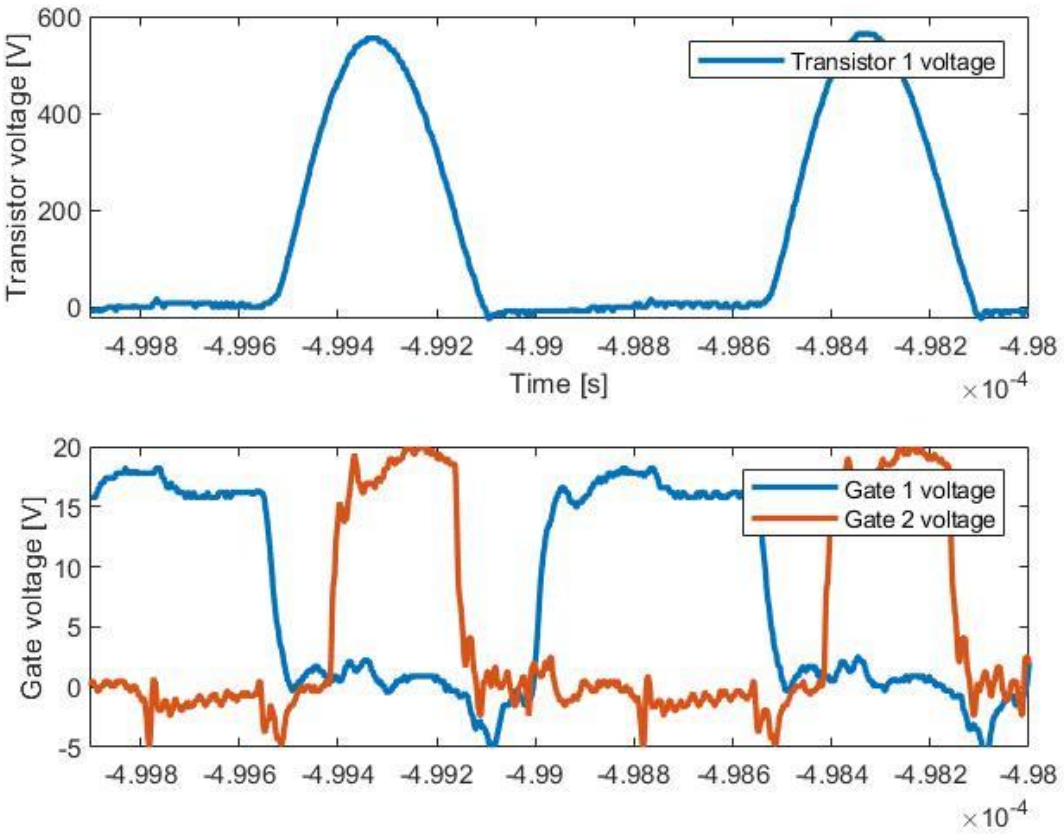

Figure 51. Drain-to-source voltage of transistor 1 and gate voltage of transistor 1 and 2 for the second suggested converter at 120 V/ 60 Hz.

7.3 Trouble shooting

The large difference between simulated values and the experimental values are investigated. When using high frequency, the parasitic effect is more prone. The resonant capacitor for the first suggested converter has been increased to offset parasitic effects from diodes in the rectifier, as these diodes appear in series with the resonant circuit. Further, the converter has been modified and tested again with new parameters to observe performance. This result is included in appendix D. During the second test, the resonant inductor was reduced, the duty cycle and switching frequency was changed and the load resistance was increased.

The inductor has been measured to 86.5 μH during design of the inductor and when connected to PCB, the inductor increased to 218.2 μH. Also, the parasitic resistance in the inductor changed. The parasitic resistance of the inductor was measured to 4 Ω during design and when connected, it increases to 68.9 Ω. During the second test of the first suggested converter, the resonance inductor was reduced from 86.4 μH to 71.85 μH.

Switching frequency and duty cycle was initially set to 1 MHz at 0.45 duty cycle and changed to 1.15 MHz at 0.43 duty cycle. The last change in front of the second test was to increase the load resistance from 401 Ω to 988 Ω. These changes improved the output voltage and efficiency from 80.2 V at 40.2 % efficiency to 259.5 V at 77.8 % efficiency, and thus, reduced the switching temperature from 101 °C to 53.9 °C. The THD decreased from 25.95 % to 22.96 % and the power factor increased from 0.93 to 0.96.

Both converters have been designed to operate as step-down voltage converters, where through the second test of the first suggested converter, the operation changed to step-up voltage and it improved the performance. This indicates that these converters shall operate as step-up voltage, and this will be further investigated as future work.

8 Conclusion

Both converters showed PFC capabilities with harmonic content within the limits of IEC 61000-3-2 for a Class C equipment. The converters achieved ZVS for the designed frequency. However, the first suggested converter gave periods of switching on at non-zero values when low drain-to-source voltage, while the second converter attain ZVS during both high and low drain-to-source voltage. Although ZVS was achieved, performance was lower than simulated values. This was investigated for the first suggested converter, and through a second test with changed parameters, the converter showed better performance compared to the first test. During the second test, the converter gave an output voltage of 259.5 V, 79.5 % efficiency, power factor of 0.96 and 22.5 % THD. Increased performance is a result of increased load resistance, increased frequency, changed duty cycle and decreased resonant inductor.

Trouble shotting and increased performance discusses the converters working as step-down converter and the effects of parasitic capacitance and inductance. To offset the parasitic effect, parasitic capacitance and inductance from diodes, switches and the PCB should be incorporated during design.

9 Future work

Future work to improve performance of converters will consist of following:

- Reiterate design.
- Debugging of PCB design.
- Transient analysis.

Reiterate the design to include the parasitic effect, incorporate the gain of the converter and for the converters to work as step-up voltage. The parasitic effects that needs to be included comes from diodes, switches, and the PCB, where the goal is to improve the efficiency of the converter for high frequency. The second converter should be redesigned with higher difference between duty cycle 1 and duty cycle 2. Equation (4,24) shows higher current gain when D_1 is high and D2 low than when they are close or equal.

Debugging of the PCB design was not completed due to lack of time. A better understanding of the parasitic effects and the operation would have increased the performance of the first converter and made it possible to test the second converter at 240 V/ 50 Hz.

By evaluating the converter from a transient perspective, the converters performance in front of steady state is better understood. This might also lead to a better understanding of the parasitic effect and how it affects the converter.

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10 Appendix

A Class-E inverter

Further mathematical relationship is expressed here. the capacitor current is found by:

$$i_{C_{S1}} = \begin{Bmatrix} 0 & 0 \le \omega_{S1}t \le 2\pi D_1 \\ I_{IN}|\sin(\omega_{IN}t)| - I_r * \sin(\omega_{S1}t + \phi_1) & ' 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{Bmatrix} \quad (A,1)$$

Substituting ZVS condition, $v_{S1}(2\pi) = 0$, substituted into (4,4), the magnitude gain of the resonant current has the following relationship:

$$I_r = \frac{I_{IN}\sin(\omega_{IN}t)\,2\pi(1-D_1)}{\cos(2\pi D_1 + \phi_1) - \cos\phi_1} \quad (A,2)$$

The voltage across the transistor and capacitor can further be written as

$$v_s(\omega_{S1}t) = \begin{Bmatrix} 0 & 0 \le \omega_{S1}t \le 2\pi D_1 \\ \frac{|I_{IN}\sin(\omega_{IN}t)|}{\omega C_{S1}}\left[\frac{(\omega_{S1}t - 2\pi D_1) + 2\pi(1-D_1)(\cos(\omega_{S1}t + \phi_1) - \cos(2\pi D_1 + \phi_1))}{\cos(2\pi D_1 + \phi_1) - \cos\phi_1}\right] & ' 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{Bmatrix} \quad (A,3)$$

Using the ZDS condition, $\frac{dv_S(2\pi)}{d(\omega_{S1}t)} = 0$, and substituting into eq X (v_S) gives the relationship between the phase angle and the duty cycle by:

$$\frac{dv_s(2\pi)}{d(\omega_{S1}t)} = \frac{1}{\omega C_{S1}}\left[\begin{matrix} I_{IN}|\sin(\omega_{IN}t)|(\omega_{S1}t - 2\pi D_1) + \\ I_r(\cos(\omega_{S1}t + \phi_1) - \cos(2\pi D_1 + \phi_1)) \end{matrix}\right] = 0$$

Substituting I_r from eq X, gives:

$$\frac{I_{IN}|\sin(\omega_{IN}t)|}{\omega_{S1}C_{S1}}\left[1 + \frac{2\pi(1-D_1)(-\sin(2\pi + \phi_1))}{\cos(2\pi D_1 + \phi_1) - \cos\phi_1}\right] = 0$$

$$\cos(2\pi D_1 + \phi_1) - \cos\phi_1 = 2\pi(1-D_1)\sin\phi_1$$

Using trigonometric identities gives:

$$\tan\phi_1 = \frac{\cos 2\pi D_1 - 1}{2\pi(1-D_1) + \sin 2\pi D_1} \quad (A,4)$$

According to [32] which states that since switching frequency is higher than the resonant frequency, ω > ω0, the current in the resonant circuit will lag the voltage across it, giving a phase-angle increase with π. The phase angle is then written as:

$$\phi_1 = \pi + \arctan\frac{\cos 2\pi D_1 - 1}{2\pi(1 - D_1) + \sin 2\pi D_1} \qquad (A,5)$$

From Eq, it is given that ϕ_1 is depending on only the duty cycle. Further, the normalized current and voltage through the transistor are given by:

$$\frac{i_S}{I_{IN}|\sin(\omega_{IN}t)|} = \begin{Bmatrix} 1 - \dfrac{2\pi(1 - D_1)\sin(\omega_{S1}t + \phi_1)}{\cos(2\pi D + \phi_1) - \cos\phi_1} & for\ 0 \le \omega_{S1}t \le 2\pi D_1 \\ 0 & , for\ 2\pi D_1 \le \omega_{S1}t \le 2\pi \end{Bmatrix} \qquad (A,6)$$

$$\frac{v_S}{V_{IN}} = \begin{Bmatrix} 0 & for\ 0 \le \omega t \le 2\pi D \\ \dfrac{\left[(\omega t - 2\pi D) + \dfrac{2\pi D(1 - D)[\cos(\omega t + \phi)]}{\cos(2\pi D + \phi) - \cos\phi}\right]}{(1 - D)[\pi(1 - D)\cos\pi D + \sin\pi D]} & , for\ 2\pi D \le \omega t \le 2\pi \end{Bmatrix} \qquad (A,7)$$

When ωt is at its maximum value, the voltage and current stress will reach its maximum value. $\omega t_{i,max}$ for current and voltage occurs at:

$$\omega_{S1}t_{i,max} = \frac{3\pi}{2} - \phi_1 \qquad (A,8)$$

$$\omega_{S1}t_{v,max} = 2\pi - \phi_1 + \arcsin\left[\frac{\cos(2\pi D_1 + \phi_1) - \cos(\phi_1)}{2\pi(1 - D_1)}\right] \qquad (A,8)$$

The expected peak voltage across the resonant inductor and capacitor is given by:

$$V_{C_r} = \frac{I_r}{\omega_{S1}C} \qquad (A,9)$$

$$V_{L_r} = \omega_{S1} * L_r * I_r \qquad (A,10)$$

B Inductor design

The given parameter for the toroidal core, $T130-2$, and Litz wire CLI 200/120 is found in table 11.

Table 11. Inductor core parameters for T130-2

Toroidal core T130-2	**Parameter**
Effective magnetic length, l_e	8,28 cm
Reference inductance, μ_i	10
Window area, W_A	2,93 cm^2
Core cross section area, A_C	0,698 cm^2
Inductance value, A_L	11 nH/N^2
Volume of core, V_{Core}	5.78 cm^3
Mean length per turn, l_{mean}	4,73 cm/N
Litz Wire CLI 200/120	
Resistance per meter, AWG 17	22 $m\Omega$/m
Cross sectional area, $A_{LitzWire}$	0.943 mm^2

The number of turns if found by:

$$N = \sqrt{\frac{A_L}{L}} \qquad (B,1)$$

The cross-sectional area of the bare winding wire given from the Litz wire:

$$Jm = \frac{I_{rms}}{A_W} \qquad (B,2)$$

The total wire length:

$$l_{TOT} = l_{mean} * N \qquad (B,3)$$

Magnetomotive fore

$$F = N * I_{Lm} \qquad (B,4)$$

Magnetic field strength

$$H = \frac{F}{l_e} = \qquad (B,5)$$

According to Micrometals, H should be lower than 200 to avoid saturation of the core. Percent of saturation of the core can be found by:

$$\mu\% = \frac{1}{10^{-2} + H^{1,14}} + 0 \qquad (B,6)$$

Expected magnetic flux strength:

$$B = \frac{V_{Lmaks}}{\sqrt{2}} * \frac{10^8}{4.44 * A_C * N * f} \qquad (B,7)$$

Where B is given in gauss. Relationship between gauss and Tesla is:

$$T = \frac{Gauss}{10\,000} \qquad (B,8)$$

Power loss in core per cubic centimeter is given by:

$$P_{Core} = \frac{f}{4 * \frac{10^9}{B^3} + 3 * \frac{10^8}{B^{2.3}} + 2.7 * \frac{10^6}{B^{1.65}}} + 9.6 * 10^{-16} * B^2 * f^2 \qquad (B,9)$$

Where power loss in core is given by:

$$P_{Core\ loss} = P_{Core} * V_{Core} \qquad (B,10)$$

The equivalent series resistance of the core is given by:

$$R_{ESR} = \frac{P_{Core\ loss}}{I_L^2} \qquad (B,11)$$

The used Litz Wire, AWG 17, has a resistance of $25\,\frac{m\Omega}{m}$, giving an DC resistance of:

$$R_{DC} = 25\frac{m\Omega}{m} * l_T \qquad (B,12)$$

MATLAB code

```
% Design parameters
VLM = 1.7e3
f=1e6
omega = 2*pi*f
Ku = 0.15
Jm = 4 % A/mm^2
Jmm = Jm * 10^6
```

```
Bm = 0.054 % mT This value is calculated below
QL = 6
L = 86.3e-6
Ln = 86.6e3 % nH
ILm = 2,8 %Expected according to simulation of Class-E Class-E is 2,79 A
Po = 300
Idc = 52e-6 %Simulated to 52 micro Ampere, according to LT spice
```

Magnetc parameters T130-2 Elfa Distrelec

```
Ac = 0.698 %cm^2
%Inner area Wa
Wa = 2.93 %cm^2
%Bandwidth >= 2MHz
ui = 10 % Insted of ur
u0 = 4*pi/10^8
%Effective magnetic length
le = 8.28
AL = 11 % nH
% Volume om core
Vc = 5.78 %cm^3
lmean = 4.73 %cm/N
```

Design of AC inductor

```
% Core area product Ap
Ap = QL*Po/(pi*Ku*Jmm*Bm*f)
Apcm = Ap*10^8
Apcore = Ac*Wa % cm^4. Apcore should be larger than Apcm


% Number of turns
N = sqrt(Ln/AL) %L in nH and AL in nH/t
Npick = 89
Aw = ILm/Jmm % m^2
Awmm = Aw*10^6 % mm^2
```

Saturation according to Micrometals

```
%Magnetomotric force
F = N*ILm
% Magnetic field strength
H = F/le
%Magnetic flux density
B = ui*u0*H


% According to Micrometals, H should be less than 200
my = 1/(1e-2+H^1.46) + 0 % Percent of saturation


Bpk = (VLM/sqrt(2)*10^8)/(4.44*Ac*N*f) % Gaus divide by 10000 to get Tesla
BT = Bpk/10000 %Tesla
```

```
%Core power loss according to Micrometals
Pc = f/(4e9/Bpk^3+3e8/Bpk^2.3+2.7e6/Bpk^1.65)+9.6e-16^2*Bpk^2*f^2 %mW / cm^3


P = Pc/1000*Vc %W/cm^3


%Equivalent Series Resistance (ESR) of the core
Rcs = 2*Pc/(ILm^2*1000) %Ohm
```

Wire Parameter

```
%length
ltotal = ceil(lmean*ceil(N))/100 % meter
RDC = 25e-3*ltotal


 % 66.2 is a constant [mm]
 %skin depth of copper at f = 1 MHz
theta = 66.2/sqrt(f)
thetaw = theta*1e3 %micro meter


Aw = 0.94 %mm^2 CLI 200/120 Letz Wire
%One single strand:
Awso = (di^2/4)/(theta^2)
di = 0.1 %mm^2 outer diameter
```

C PCB Assembly drawing

The Assembly drawing of the first suggested converter, the second suggested converter and the current measure PCB.

The first suggested converter

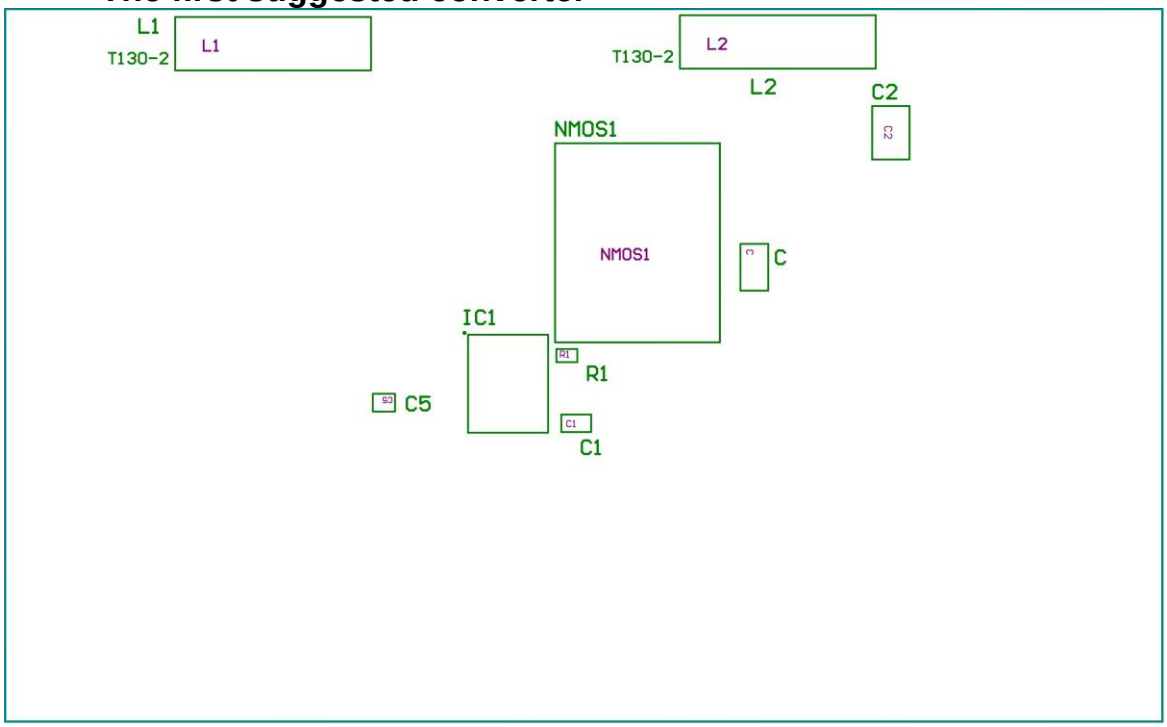

Figure 52. Top layer of the first suggested converter.

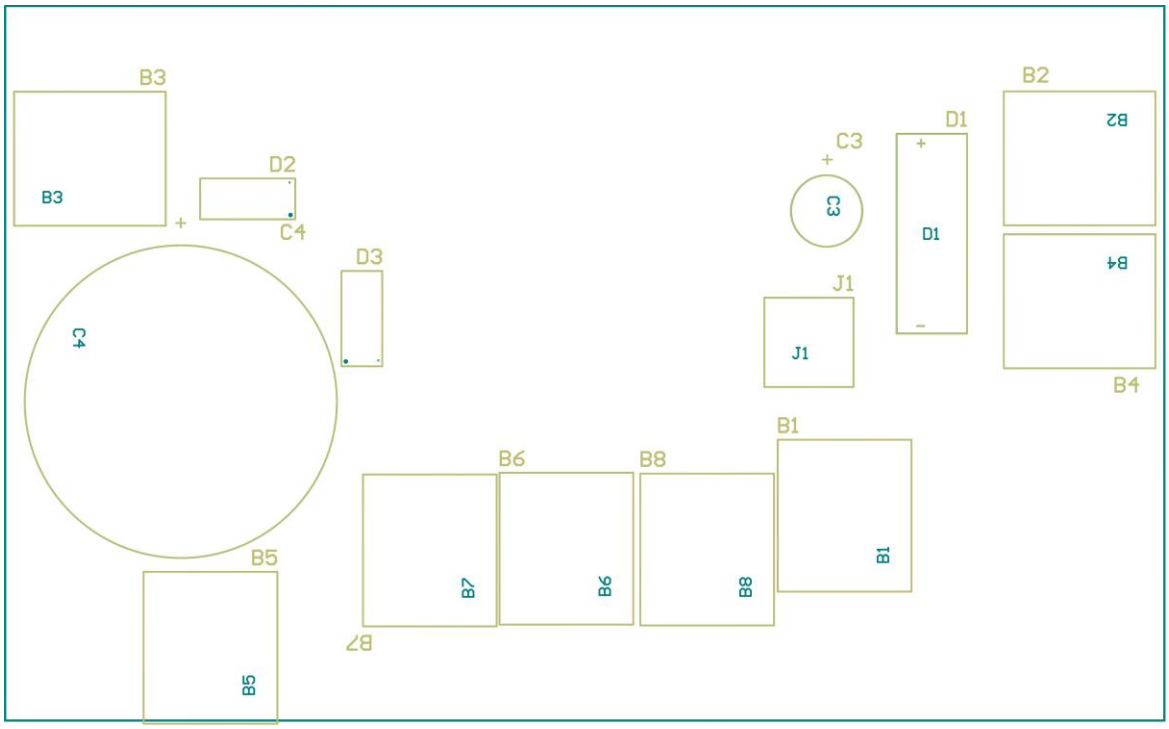

Figure 53. Bottom Layer of the first suggested converter.

The second suggested converter

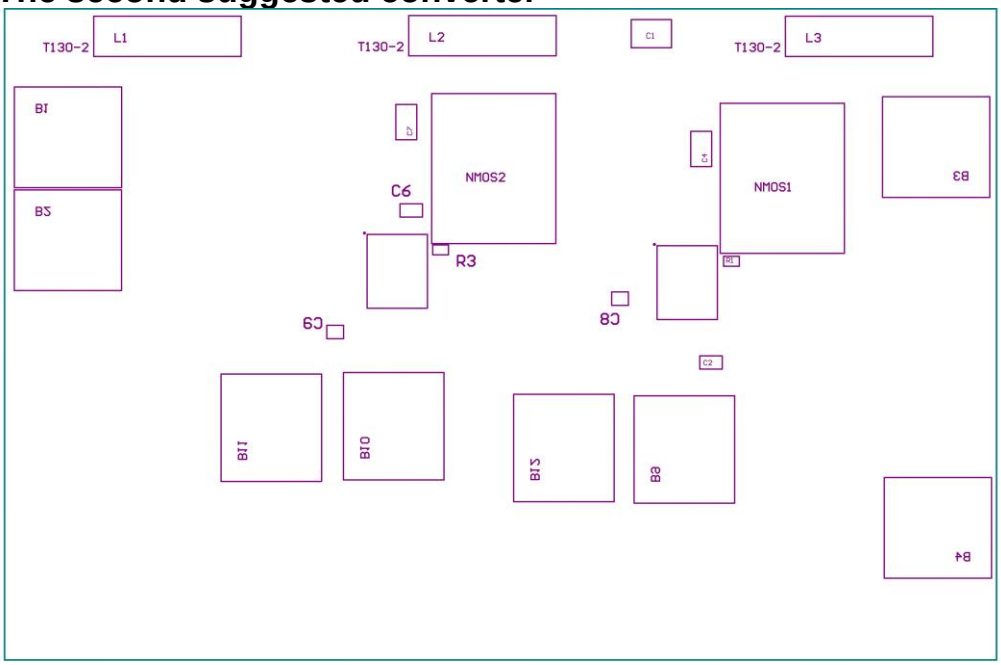

Figure 54. Top layer of the second suggested converter.

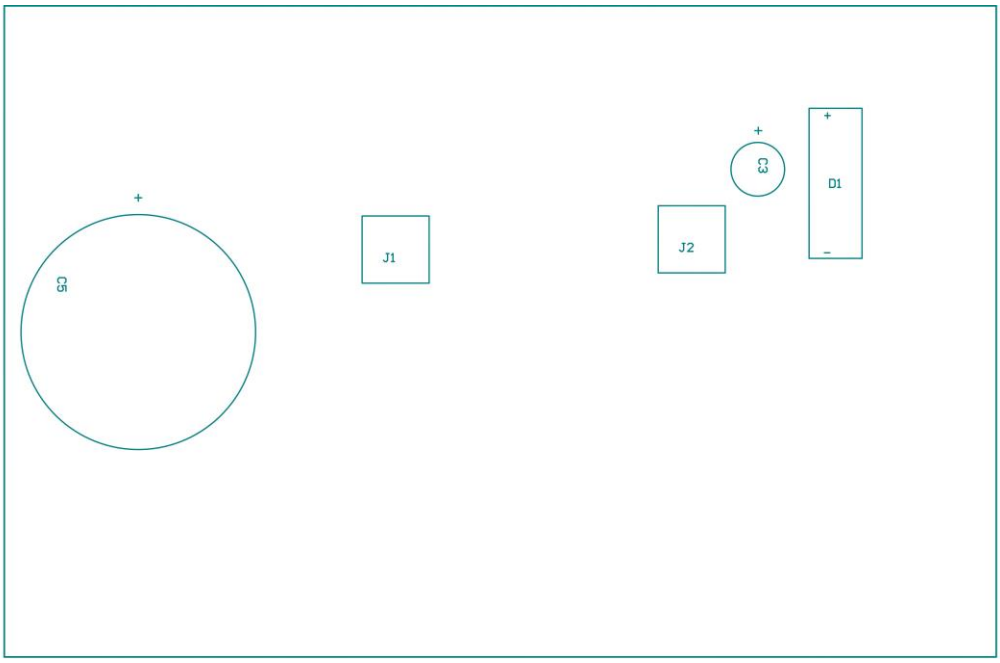

Figure 55. Bottom layer of the second suggested converter

Current measure PCB

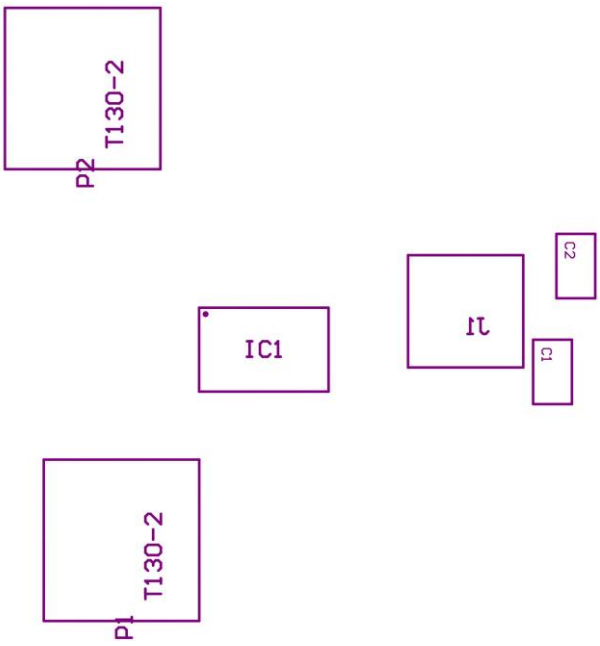

Figure 56. Top layer of current measure PCB.

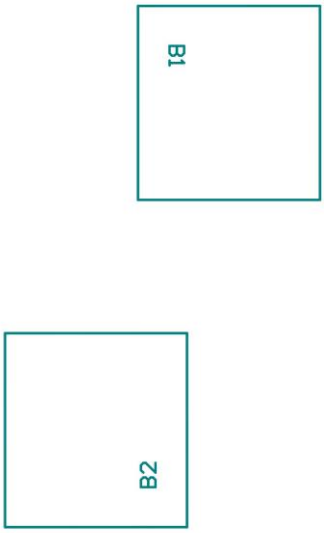

Figure 57. Bottom layer of current measurement PCB.

D Second test of the first suggested converter

The testing is conducted with applied voltages from 85 V- 240 V with line frequency of 50 Hz and 120 V at 60 Hz, where 240 V/ 50 Hz and 120 V/60 Hz is evaluated. Component values and switching frequency used though the experiment is found in table 12.

Table 12. Component values through second test

Component	Second test component values
Input capacitor, C_{IN}	1 µF
Load resistance, R_L	988 Ω
Resonant inductor, L_r	71.85 µH
Shunt capacitor, C_S	220 pF
Resonant capacitor, C_r	580 pF
Inductor, L_{IN} and L_{OUT}	1 mH
Filter capacitor, C_F	560 µF
Frequency	
Frequency	1.15 MHz

240 Voltage at 50 Hz

Figure 58 shows the grid voltage, grid current and the output voltage of the converter. The figure shows an output average voltage of $259.5\,V$ and a rms value of the grid current of $0.34\,A$.

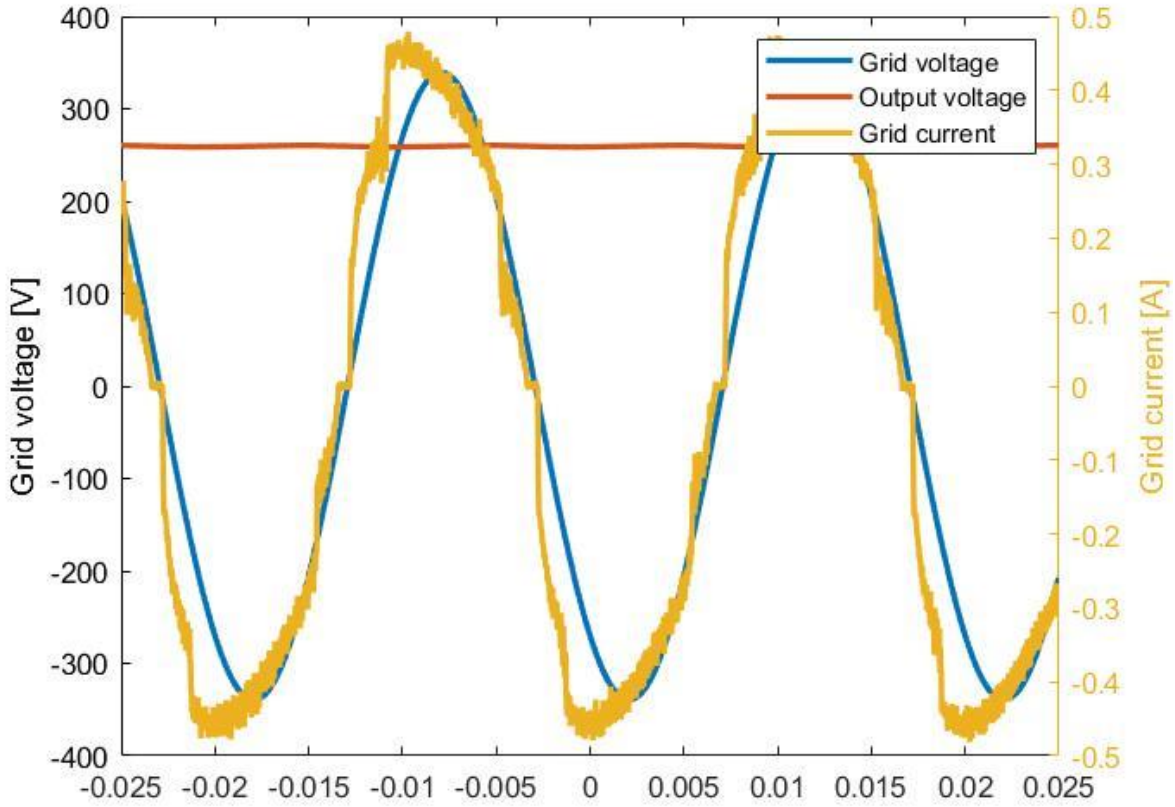

Figure 58. Grid voltage, output voltage and grid current for the first suggested converter at the second test for 240 V/ 50 Hz.

Figure 59 shows harmonic distortion of the current, harmonic limits for a Class C equipment and input and output power. The harmonic content is measured in the grid current from the fundamental frequency and up to the 40^{th} harmonics and plotted against the limits of Class C equipment according to IEC 61000-3-2. THD and PF are $22.96\,\%$ and 0.96, where the fundamental frequency is $50\,Hz$. The efficiency of the converter is measured to $79.5\,\%$, with an average input power of $79\,W$ and an average output of $62\,W$.

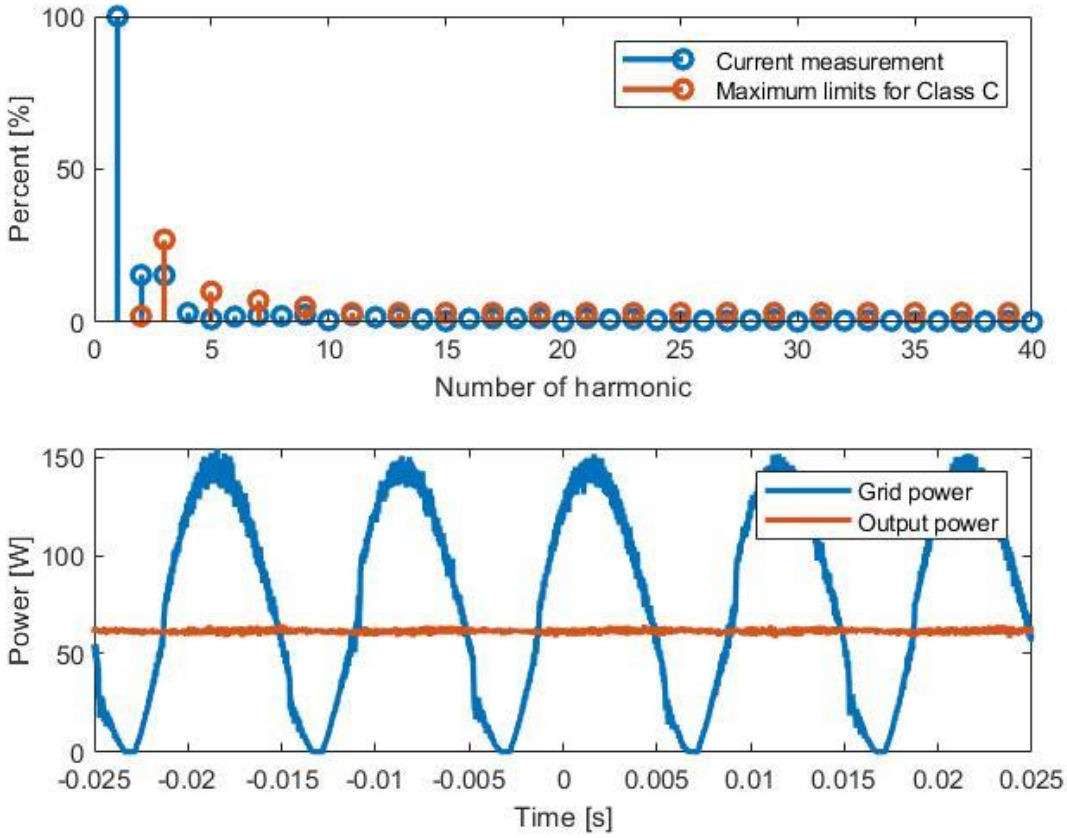

Figure 59. Harmonic content, maximum limits for Class C equipment according to IEC 61000-3-2 and power tested for the first converter at the second test.

Figure 60 shows the drain-to-source voltage across the transistor and transistor gate voltage over a switching cycle, and the drain-to-source voltage across one line cycle. Suboptimal operation is shown by the slope of the switch voltage, and that the switch voltage drops below zero.

Alignment of the two plotted graphs does makes it hard to see the operation condition. Suboptimum operation indicates that the load resistor is lower than the optimum resistor. Still, it is higher than the calculated values. Affected by parasitic effects from the circuit. During the periods with low voltage across, the same behaviour as seen in figure 31 occur. However, this effect is not as prone with the chosen parameter and not visible on the figure as of as low numbers of plots from the oscilloscope. The peak values of the drain-to-source voltage across the line cycle shows a voltage stress lower than the simulated and calculated values.

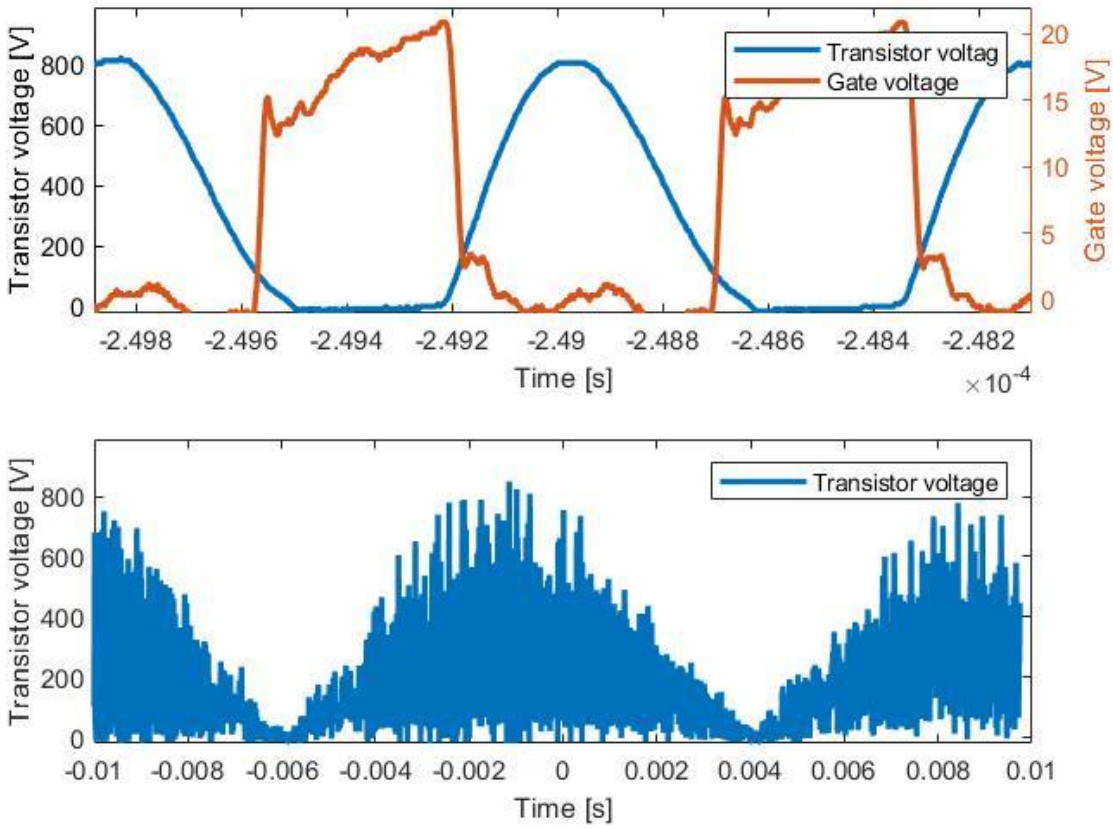

Figure 60. Drain-to-source and gate voltage across switching cycles and drain-to-source voltage across line cycle for the first converter at the second test for 240 V/ 50 Hz.

Figure 61 shows the temperature of the transistor during the second testing of the first suggested converter. It shows a low transistor temperature indicating low switching losses.

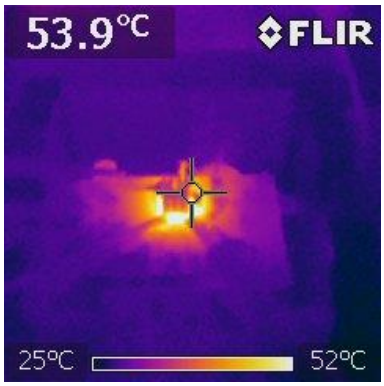

Figure 61. Temperature during the second test of the first suggested converter at 240 V/ 50Hz.

120 Voltage at 60 Hz

Figure 62 shows grid voltage, grid current and the output voltage of the converter at 120 V / 60 Hz. The average output voltage is 124.1 V and the RMS value of the grid current is 0.17 A.

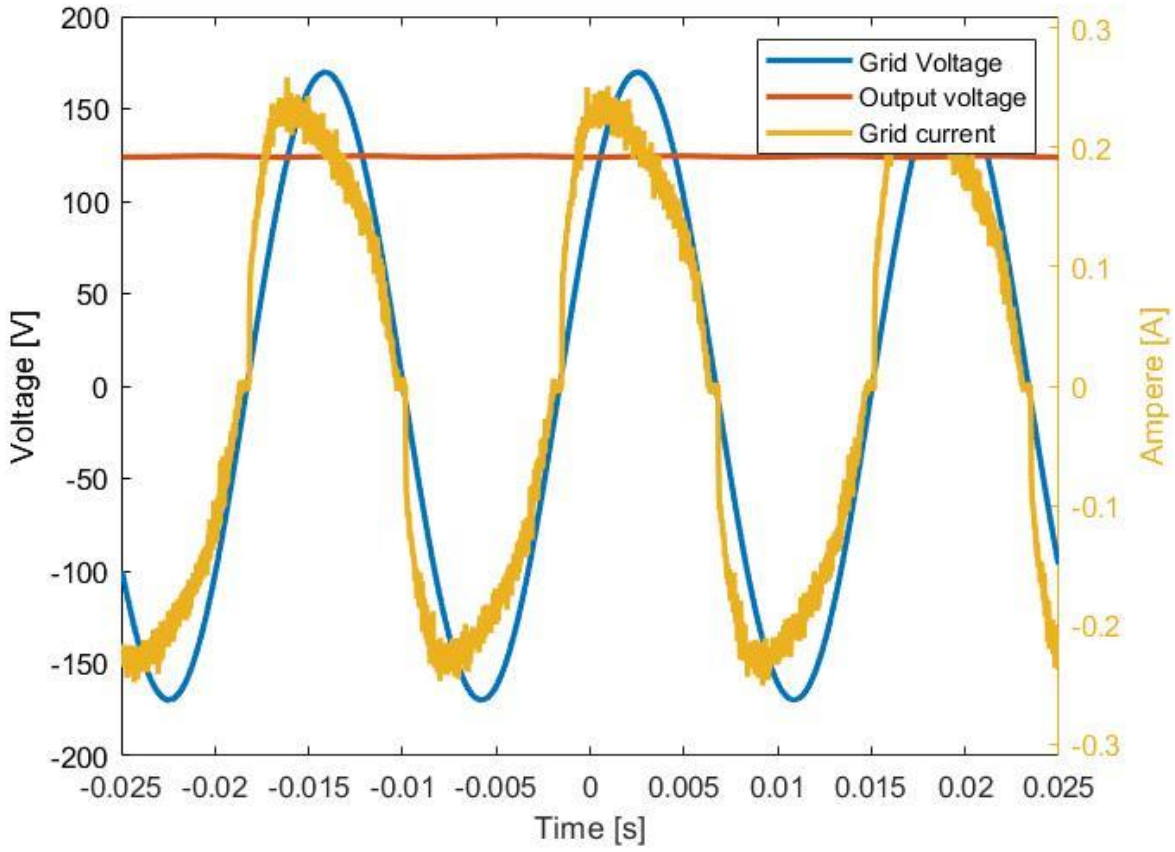

Figure 62. Grid voltage, output voltage and grid current for the first suggested converter at the second test of 120 V/ 60 Hz.

Figure 63 shows harmonic distortion of the grid current, harmonic limits for a Class C equipment according to IEC 61000-3-2 and input and output power. The harmonic content is measured in the grid current from the fundamental frequency and up to the 40^{th} harmonics and plotted against the limits of Class C equipment. THD and PF are 18.51 % and 0.952 where the fundamental frequency is $60\ Hz$. The efficiency of the converter is measured to 77.7%, and the average input power $20\ W$ and an average output of $16\ W$.

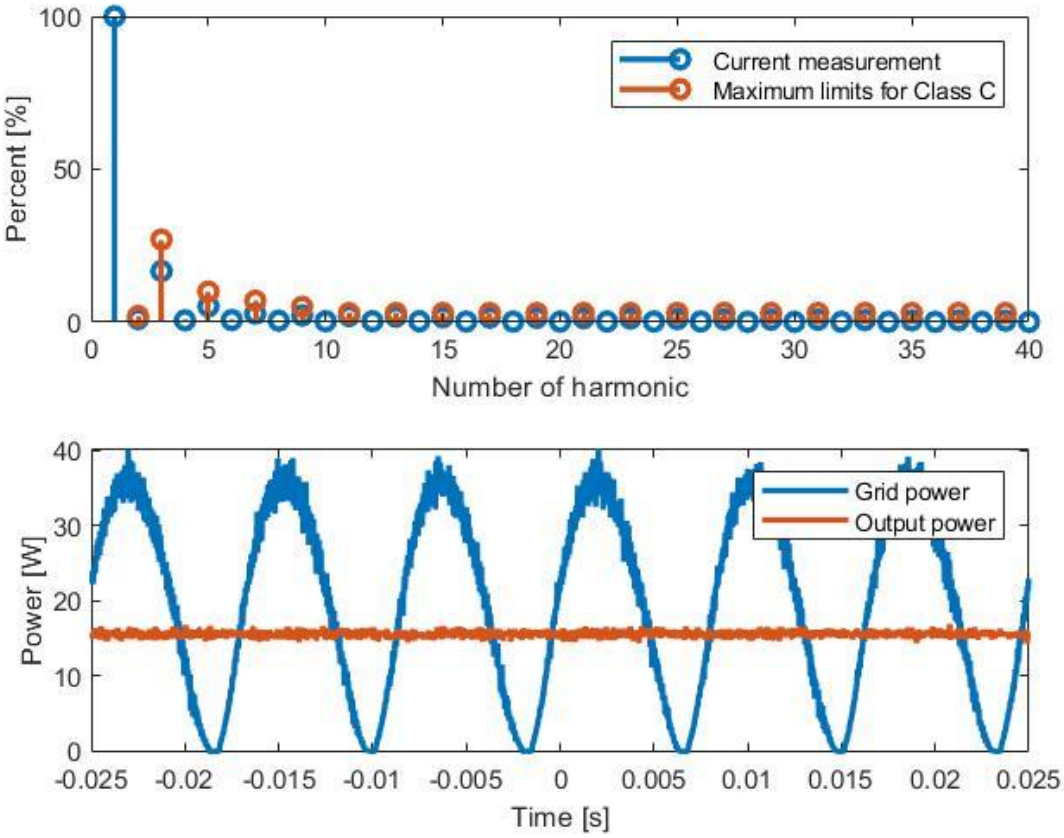

Figure 63. Harmonic content, maximum limits for Class C equipment according to IEC 61000-3-2 and power tested for the first converter at the second test for 120 V/ 60 Hz.

Figure 64 shows the drain-to-source voltage across the transistor plotted with the gate voltage over two periods of switching cycles and one period of line cycle. This parameter gave also suboptimal operation, shown by the slope and negative drain-to-source voltage, equal to figure 60.

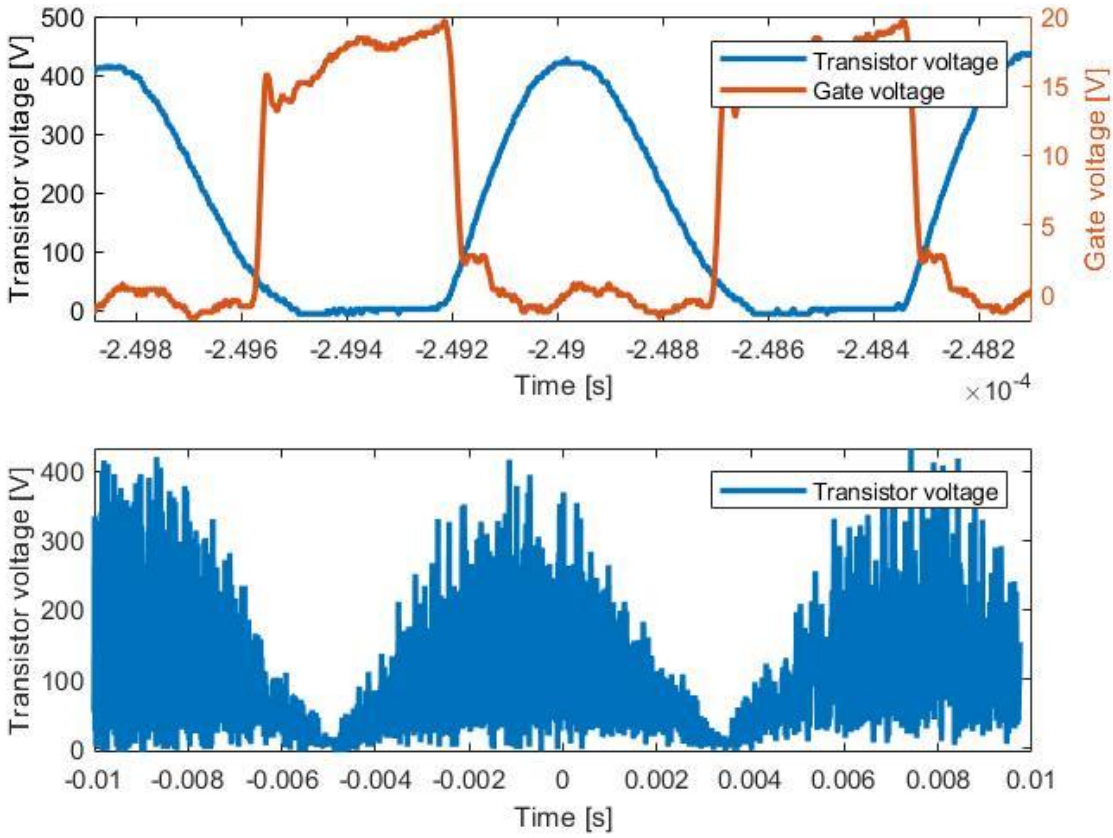

Figure 64. Drain-to-source and gate voltage across switching cycles and drain-to-source voltage across line cycle for the first converter at the second test for 120 V/ 60 Hz.

Figure 65 shows the temperature of the transistor during the second testing of the first suggested converter. The figure showed lower temperature during the second test compare to the first test for the same applied voltage.

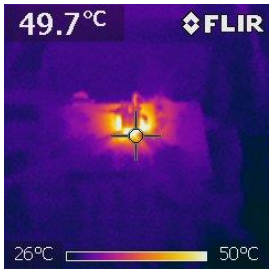

Figure 65. Temperature during the second test of the first suggested converter 120 V/ 60Hz.

E MATLAB code for converter design

Converter calculations

```
Vi = 240; % Input voltage [V]
Pri = 300; %Highest output power [Watt]
fl = 50;
f = 0.9e6; % Switching frequency [MHz]
% Vo=200;
omega = 2*pi*f
omegal = 2*pi*fl;
D2 = 0.45;


phi2 = pi + atan((cos(2*pi*D2)-1)./(2*pi*(1-D2)+sin(2*D2*pi)))
phid = phi2*180/pi


omegaC1Ri2 = (2*sin(pi*D2)*cos(pi*D2+phi2)*sin(pi*D2+phi2)*...
    ((1-D2)*pi*cos(pi*D2)+sin(pi*D2))./(pi^2*(1-D2))
wt_im2 = (3*pi/2) - phi2
wt_vm3 = 2*pi - phi2 + asin((cos(2*pi*D2+phi2)-cos(phi2))/(2*pi*(1-D2)))
%The full load resistance is
Ri = (2*(sin(pi*D2))^2*(sin(pi*D2+phi2))^2*Vi^2)/(pi^2*(1-D2)^2*Pri)
%Reflected to the rectifier
RL = Ri*pi^2/2
%The DC resistance of the inverter is
RDC = ((1-D2)*(pi*(1-
D2)*cos(pi*D2)+sin(pi*D2)))/(omegaC1Ri2*tan(pi*D2+phi2)*sin(pi*D2))*Ri
%Amplitude of the output voltage
VRim = - (2*sin(pi*D2)*sin(pi*D2+phi2))/(pi*(1-D2))*Vi
Po = VRim^2/(2*Ri)
%The Maximum voltage across the switch and the shunt capacitor can be
calculated
Vsm = ((tan(pi*D2+phi2).*sin(pi*D2))./((1-D2).*((pi*(1-
D2).*cos(pi*D2))+sin(pi*D2))))...
    .*((wt_vm3-2*pi*D2)+((2*pi*(1-D2)).*(cos(wt_vm3+phi2)-
cos(2*pi*D2+phi2)))./...
    (cos(2*pi*D2+phi2)-cos(phi2)))*Vi
%DC input current is
Ii = Vi/RDC
%The maximum switched current obtained
Ism = (1-((2*pi*(1-D2).*sin(wt_im2+phi2))./(cos((2*pi*D2)+phi2)-
cos(phi2))))*Ii
%The amplitude of the current through the resosnatn circuit
Im = (2*pi*(1-D2))/(cos(2*pi*D2+phi2)-cos(phi2))*Ii
%Assuming QL is 6. It is important to have Q1 >= 5
QL = 6;
L = QL*Ri/omega
C1 = (2*sin(pi*D2)*cos(pi*D2+phi2)*sin(pi*D2+phi2)*((1-
D2)*pi*cos(pi*D2)+sin(pi*D2)))./...
        (pi^2*(1-D2)*omega*Ri)

%Finding Lb
```

```
Lb = (2*((1-D2)^2)*(pi^2)-1+2*cos(phi2)*cos(2*pi*D2+phi2)-
cos(2*(pi*D2+phi2))*(cos(2*pi*D2)-pi*(1-
D2)*sin(2*pi*D2))./(4*sin(pi*D2)*cos(pi*D2+phi2)*sin(pi*D2+phi2)*((1-
D2)*pi*cos(pi*D2)+sin(pi*D2))) *Ri/omega
%Capacitor
C = 1/(Ri*QL*omega-omega^2*Lb)
%Input and output inductor
Lfmin = 2*((pi^2/4+1)*Ri/f)
%The peak voltage across resonant capasitor C and inductor L are
Vcm = Im/(omega*C)
VLm = omega*L*Im

%Assuming that the DC ESR of the choke Lf is rLf = 0.15 Ohm.
% Then the power loss in the inductor is
PrLf = 0.15*Ii^2 %Watt

%The rms value of the switch current is
fun = @(theta1) ((pi/2*sin(theta1)-cos(theta1)+1)*Ii).^2
ISrms = sqrt(1/(2*pi)*integral(fun,0,pi)) %Ampere

%If the MOSFET used has a on-resistance rDS =1 Ohm, the transistor
%conduction power loss is
PrDS = 1*ISrms^2 %Watt lost in on-state

% rms current through the shunt capacitor
fun2 = @(theta2) ((pi/2*sin(theta2)-cos(theta2)+1)*Ii).^2
IC1rms = sqrt(1/(2*pi)*integral(fun2,pi,2*pi))

% Capacitor for a maximum voltage ripple of 2%
Cf = Pri/(.04*omegal*200^2*n/100)
```

The second suggested converter gain

```
%D1 = x and D2 = y
 [x,y] = meshgrid(0.1:0.01:1,0.1:0.01:1);
Io2Ig = ((1-x).*(cos(2*pi*y+(pi + atan((cos(2*pi*y)-1)./(2*pi*(1-
y)+sin(2*pi*y)))))-...
    cos(pi + atan((cos(2*pi*y)-1)./(2*pi*(1-y)+sin(2*pi*y)))))./((1-
y).*(cos(2*pi*x...
    +(pi + atan((cos(2*pi*x)-1)./(2*pi*(1-x)+sin(2*pi*x)))))-cos(pi +
atan((cos(2*pi*x)-1)./(2*pi*(1-x)+sin(2*pi*x))))));


% Plotting of Gain
figure
surf(x,y,Io2Ig),view(45,30)
zlim([0 5])
title('Current gain as function of duty cycle D_1 and D_2')
xlabel('Duty cycle 1')
ylabel('Duty cycle 2')
zlabel('Current gain')
```

Plotting stress

```
%Ploting the switching stress curve
Ds = 0:0.01:1;
DD = 0:0.01:1;
for i = 1:101
phip(i) = pi + atan((cos(2*pi*Ds(i))-1)./(2*pi*(1-Ds(i))+sin(2*Ds(i)*pi)));
phip2 (i) = pi + atan((cos(2*pi*Ds(i))-1)/(2*pi*(1-Ds(i))+sin(2*pi*Ds(i))));
dphi(i) = rad2deg(pi + atan((cos(2*pi*Ds(i))-1)/(2*pi*(1-
Ds(i))+sin(2*pi*Ds(i)))));
dphi2 (i) = rad2deg(phip2 (i));
wt_im(i) = (3*pi/2) - phip(i);
wt_vm(i) = 2*pi - phip(i) + asin((cos(2*pi*Ds(i)+phip(i))-
cos(phip(i)))/(2*pi*(1-Ds(i))));
Ism2Iin(i) = 1-((2*pi*(1-
Ds(i)).*sin(wt_im(i)+phip(i))./(cos((2*pi*Ds(i))+phip(i))-cos(phip(i))));
Vsm2Vin(i) = ((tan(pi*Ds(i)+phip(i)).*sin(pi*Ds(i))./((1-Ds(i)).*((pi*(1-
Ds(i)).*cos(pi*Ds(i)))+sin(pi*Ds(i)))))...
    .*((wt_vm(i)-2*pi*Ds(i))+((2*pi*(1-Ds(i))).*(cos(wt_vm(i)+phip(i))-
cos(2*pi*Ds(i)+phip(i)))./...
    (cos(2*pi*Ds(i)+phip(i))-cos(phip(i))));
Cp (i) = 1/(Ism2Iin(i)*Vsm2Vin(i));
%Output current gain as function of duty cycle
% Io2Ig(i) = (1-Ds(i)*(cos(2*pi*DD(i)+phip(i))-cos(phip2(i))))/((1-
DD(i))*(cos(2*pi*Ds(i)+phip(i))-cos(phip(i))));


end


figure
plot(Ds,phip2)
% axis([0,1,90,180])
title ('Phase angle as a funaction of duty cycle')
ylabel ('Angle')
xlabel('Duty cycle')
ax = gca;
chart = ax.Children(1);
datatip(chart,0.45,152.6);




figure
plot(Ds,dphi)
hold on
plot(Ds, dphi2)
axis([0,1,90,180])
title ('Phase angle as a funaction of duty cycle')
ylabel ('Angle')
xlabel('Duty cycle')
ax = gca;
chart = ax.Children(1);
```

```
datatip(chart,0.45,152.6);


figure
plot(Ds, Ism2Iin)
hold on
plot(Ds, Vsm2Vin)
title('Normalized switch peak values')
legend('Ism/I_I', 'Vsm/V_I')
xlabel('duty cycle')
ylabel('Normalized switch peak value')
axis([0 1 0 10])


figure
plot(Ds,Cp)
title('Power capability')
ylabel('Power capability')
xlabel('duty cycle')
```

F MATLAB code for simulated result

MATLAB code for simulation of the first and the second suggested converter.

First suggested converter

The first suggested converter

```
clear
 ClassD = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Simualtion\ClassEClassD22.txt');
ClassD2 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Simualtion\ClassEClassD2highshuntcap.txt');
```

```
t = ClassD(:,1);
Vgrid =ClassD(:,2);
Pin = ClassD(:,3);
Pout = ClassD(:,4);
Vout = ClassD(:,5);
Vgate = ClassD(:,6);
Vswitch= ClassD(:,7);
Ires = ClassD(:,8);
ILin = ClassD(:,9);
IRL = ClassD(:,10);
Igrid = (-1).*ClassD(:,11);
Iswitch= ClassD(:,12);
t2 = ClassD2(:,1);
Vgrid2 =ClassD2(:,2);
Pout2 = ClassD2(:,3);
Vout2 = ClassD2(:,4);
Vgate2 = ClassD2(:,5);
Vswitch2 = ClassD2(:,6);
IRL2= ClassD2(:,7);
```

```
Igrid2 = ClassD2(:,8);
Iswitch2 = ClassD2(:,9);
```

```
IgridRMS = rms(Igrid)
avgVout = mean(Vout, 'omitnan')
avgIres = mean(Ires, 'omitnan')
avgPout= avgVout*avgIres
meanPout = mean(Pout, 'omitnan')
meanPin = mean(Pin, 'omitnan')


%Grid voltage, output voltage and grid current
figure
% tiledlayout(2,1)
% nexttile
plot(t,Vgrid, "LineWidth",2)
xlim([0 0.02])
% ylim([-400 400])
hold on
plot(t,Vout, "LineWidth",2)
ylabel('Voltage [V]')
yyaxis right
plot(t, Igrid, "LineWidth",2)
plot(t, ILin,'-g', "LineWidth",2)
ylabel('Ampere [A]')
% title('Grid and output voltage')
legend('Grid voltage', 'Output voltage', 'Grid current', 'Input inductor
current')
% legend box off
ylabel('Voltage [V]')
xlabel('Time [s]')
xlim([0 0.02])


%Drain-source voltage switching cycle
figure
tiledlayout(3,1)
nexttile
plot(t, Vswitch, 'LineWidth', 2)
legend('Drain-source voltage')
ylabel('voltage [V]')
xlim([4.9995e-3 5.001e-3])
ylim([-200 1700])
xlabel('Time [s]')


nexttile
plot(t,Vgate, "LineWidth", 2)
legend('Gate voltage')
% legend box off
% title('Gate voltage')
```

```
ylabel('Voltage [V]')
xlim([4.9995e-3 5.001e-3])
ylim([-2 20])
xlabel('Time [s]')


nexttile
plot(t, Iswitch, 'LineWidth', 2)
% title('Drain-to-source voltage')
legend('Drain-source current')
% legend box off
ylabel('Ampere [A]')
xlim([4.9995e-3 5.001e-3])
% ylim([-200 1700])
xlabel('Time [s]')




figure
tiledlayout(2,1)
nexttile
plot(t, Ires, 'LineWidth',2)
hold on
plot(t, ILin, 'LineWidth',2)
xlim([0 0.02])
% title('Resonant and input current')
ylabel('Ampere [A]')
legend('Resonant current', 'Input inductor current')
xlabel('Time [s]')
nexttile
plot(t, Igrid)
hold on
plot(t, ILin)
xlim([0 0.02])
% title('Grid and input current')
ylabel('Ampere [A]')
legend('Grid current', 'Input inductor current')
xlabel('Time [s]')

%Resonant inductor vs. input inductor
figure
tiledlayout(2,1)
nexttile
plot(t2, Vswitch2, 'Linewidth', 2)
hold on
plot(t, Vswitch, 'LineWidth',2)
legend('Drain-source voltage, 220 pF', 'Drain-source voltage, 270 pF')
% legend box off
xlim([0 0.02])
% title('Drain-to-source voltage')
ylabel('Voltage [V]')
xlabel('Time [s]')
nexttile
```

```
plot(t, Iswitch, 'LineWidth',2)
hold on
plot(t2, Iswitch2, 'Linewidth', 2)
legend('Drain-source-current, 270 pF', 'Drain-source-current, 220 pF')
% legend box off
xlim([0 20e-3])
% title('Drain-to-source current')
ylabel('Ampere [A]')
xlabel('Time [s]')
```

Drain-source voltage during low voltage

```
figure
tiledlayout(3,1)
nexttile
plot(t,Vgate, "LineWidth", 2)
legend('Gate voltage')
% legend box off
% title('Gate voltage')
ylabel('Voltage [V]')
xlim([9.2948e-3 9.2968e-3])
ylim([-2 20])
xlabel('Time [s]')
nexttile
plot(t, Vswitch, 'LineWidth',2)
legend('Drain-source voltage')
% legend box off
xlim([9.2948e-3 9.2968e-3])
ylim([-50 330])
% title('Drain-to-source voltage')
ylabel('Voltage [V]')
xlabel('Time [s]')
nexttile
plot(t, Iswitch, 'LineWidth',2)
legend('Drain-source-current')
% legend box off
xlim([9.2948e-3 9.2968e-3])
ylim([-0.5 2.6])
% title('Drain-to-source current')
ylabel('Ampere [A]')
xlabel('Time [s]')
```

ZVS capability at low voltage

```
figure


plot(t, Vswitch, 'LineWidth',2)
% legend box off
xlim([8.6014e-3 8.6032e-3])
hold on
plot(t2, Vswitch2, 'Linewidth', 2)
% title('Drain-to-source voltage')
ylim([-60 600])
```

```
ylabel('Voltage [V]')
yyaxis right
plot(t, Vgate, 'LineWidth', 2)
ylim([-2 20])
ylabel('Voltage [V]')
xlabel('Time [s]')
xlim([8.6014e-3 8.6032e-3])
legend('Drain-to-source voltage, 220 pF', 'Drain-to-source voltage, 270 pF',
'Gate voltage')
```

Second suggested converter

```
clear
ClassE452 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Simualtion\ClassEClassE3.txt');
ClassE3220pF = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Simualtion\ClassEClassE3220pF.txt');
```

```
t3 = ClassE452(:,1);
Vgrid3 = ClassE452(:,2);
Pin3 =ClassE452(:,3);


Pout3 =ClassE452(:,4);


Vout3 = ClassE452(:,5);
Vgate13 = ClassE452(:,6);
Vgate23= ClassE452(:,7);
Vswitch13 = ClassE452(:,8);
Vswitch23 = ClassE452(:,9);
Ilr3 = ClassE452(:,10);
ILin3= ClassE452(:,11);
ILout3= ClassE452(:,12);
IRL3 = ClassE452(:,13);


Igrid3 = (-1)*ClassE452(:,14);
IS13 = ClassE452(:,15);
IS23 = ClassE452(:,16);


t4 = ClassE3220pF(:,1);
Vgrid4 = ClassE3220pF(:,2);
Vout4 = ClassE3220pF(:,3);
Vgate14 =ClassE3220pF(:,4);
Vgate24 = ClassE3220pF(:,5);
Vswitch14 = ClassE3220pF(:,6);
Vswitch24 = ClassE3220pF(:,7);
ILin4 = ClassE3220pF(:,8);
```

```
ILout4 = ClassE3220pF(:,9);
Iout4 = ClassE3220pF(:,10);
Igrid4 = ClassE3220pF(:,11);
IS14 = ClassE3220pF(:,12);
IS24 = ClassE3220pF(:,13);
```

```
Igrid3RMS = rms(Igrid3)
avgVout3 = mean(Vout3, 'omitnan')
avgILout3 = mean(ILout3, 'omitnan')
avgPout= avgVout3*avgILout3
meanPout3 = mean(Pout3, 'omitnan')
meanPin3 = mean(Pin3, 'omitnan')


Grid voltage, output voltage and grid current

figure
% tiledlayout(2,1)
% nexttile
plot(t3,Vgrid3, "LineWidth",2)
xlim([0 0.02])
% ylim([-400 400])
hold on
plot(t3,Vout3, "LineWidth",2)
ylabel('Voltage [V]')
yyaxis right
plot(t3, Igrid3, "LineWidth",2)
ylabel('Ampere [A]')
% title('Grid  and output voltage')
legend('Grid voltage', 'Output voltage', 'Grid current')
% legend box off
xlabel('Time [s]')

Grid current, Input inductor current and output inductor current

figure
% tiledlayout(2,1)
% nexttile
plot(t3,Igrid3, "LineWidth",2)
xlim([0 0.02])
% ylim([-400 400])
hold on
plot(t3,ILin3, "LineWidth",2)
% ylabel('Voltage [V]')
% yyaxis right
plot(t3, ILout3, "LineWidth",2)
ylabel('Ampere [A]')
% title('Grid  and output voltage')
legend('Grid current', 'Input inductor current', 'Output inductor current')
% legend box off
xlabel('Time [s]')
```

```
Drain-source voltage, gate voltage and drain-source current

figure
tiledlayout(3,1)
nexttile
plot(t3, Vswitch13, 'LineWidth', 2)
hold on
plot(t3, Vswitch23, 'LineWidth', 2)
% title('Drain-to-source voltage')
legend('Transistor 1 voltage', 'Transistor 2 voltage')
ylabel('voltage [V]')
xlim([4.9995e-3 5.001e-3])
ylim([-200 1700])
xlabel('Time [s]')


nexttile
plot(t3,Vgate13, "LineWidth", 2)
hold on
plot(t3,Vgate23, "LineWidth", 2)
legend('Transistor 1 voltage', 'Transistor 2 voltage')
% title('Gate voltage')
ylabel('Voltage [V]')
xlim([4.9995e-3 5.001e-3])
ylim([-2 20])
xlabel('Time [s]')


nexttile
plot(t3, IS13, "LineWidth",2)
hold on
plot(t3,IS23, 'Linewidth',2)
% hold on
% plot(t, ILin)
legend('Transistor 1', 'Transistor 2')
ylabel('Current [A]')
xlabel('Time [s]')
xlim([4.9995e-3 5.001e-3])
```

Difference in drain-source voltage when shunt capacitor of 220 pF and 270 pF

```
figure
tiledlayout(2,1)
nexttile
plot(t3, Vswitch23, 'LineWidth',2)
hold on
plot(t3, Vswitch13, 'LineWidth',2)
```

```
legend('Transistor 2 voltage', 'Transistor 1 voltage')
xlim([0 0.02])
% title('Drain-to-source voltage')
ylabel('Voltage [V]')
xlabel('Time [s]')
nexttile
plot(t3, IS13, 'LineWidth',2)
hold on
plot(t3, IS23,  'LineWidth',2)
xlim([0 20e-3])
legend('Transistor 1 current','Transistor 2 current')
% title('Drain-to-source current')
ylabel('Ampere [A]')
xlabel('Time [s]')
```

Difference in drain-source voltage when shunt capacitor of 220 pF and 270 pF

```
figure
tiledlayout(2,1)
nexttile
plot(t4, Vswitch14, 'LineWidth',2)
hold on
plot(t3, Vswitch13, 'LineWidth',2)
legend('Transistor 1 voltage, 220 pF', 'Transistor 1 voltage, 270 pF')
xlim([4.9995e-3 5.001e-3])
% ylim([1520 1550])
% title('Drain-to-source voltage')
ylabel('Voltage [V]')
xlabel('Time [s]')
nexttile
plot(t4, Vswitch24, 'LineWidth',2)
hold on
plot(t3, Vswitch23, 'LineWidth',2)
xlim([4.9995e-3 5.001e-3])
% ylim([1000 1500])
legend('Transistor 2 voltage, 220pF','Transistor 2 current voltage, 270 pF')
% title('Drain-to-source current')
ylabel('Voltag [V]')
xlabel('Time [s]')
```

ZVS when low drain-source voltage

```
figure
tiledlayout(2,1)
nexttile
plot(t3,Vswitch13, "LineWidth",2)
xlim([9.9990e-3 10.001e-3])
hold on
ylabel('Voltage [V]')
yyaxis right
```

```
plot(t3, Vgate13,  "LineWidth",2)
ylabel('Voltage [V]')
legend('Transistor 1 voltage', 'Gate 1 voltage')
nexttile
plot(t3,Vswitch23, "LineWidth",2)
xlim([9.9990e-3 10.001e-3])
ylabel('Voltage [V]')
hold on
yyaxis right
plot(t3, Vgate23, "LineWidth",2)
ylabel('Voltage [V]')
% title('Grid  and output voltage')
legend('Transistor 2 voltage', 'Gate 2 voltage')
% legend box off
xlabel('Time [s]')
```

ZVS when low drain-source voltage

```
figure
plot(t3,Vswitch13, "LineWidth",2)
xlim([9.9990e-3 10.001e-3])
hold on
plot(t3,Vswitch23, "LineWidth",2)
ylabel('Voltage [V]')
yyaxis right
plot(t3, Vgate13,  "LineWidth",2)
plot(t3, Vgate23,'-g',  "LineWidth",2)
ylabel('Voltage [V]')
legend('Transistor 1 voltage','Transistor 2 voltage', 'Gate 1 voltage', 'Gate
2 voltage')
xlabel('Time [s]')
```

G MATLAB code for experimental results

MATLAB code for experimental results of the first and the second suggested converter.

The first suggested converter

```
GS230 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD
580pF\ac230lassd580pf7.csv');
VC230 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\ac230 classD
580pF3.csv');


GS120 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\120V Class
d\ac120lassd580pf4.csv');
VC120 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\120V Class d\ac120
classD 580pF1.csv');
```

```
VC1202 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\120V Class d\AC120
580pF classD9.csv');


GS240 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\240V Class
d\ac240_classd_580pf.csv');
VC240 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\240V Class d\AC240
ClassD 580pF.csv');
THD240 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\240V Class d\AC240
ClassD 580pF4.csv');


standard2 = [nan 2 27 nan 10 nan 7 nan 5 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3
nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan]'


GS2402 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\240V Class
d\ac240_classd_580pf3.csv');
GS2403 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassD 580pF\240V Class
d\ac240_classd_580pf11.csv');
```

```
%240 Voltage at 50Hz
tV240 = GS240(:,1);
VSwitch240 = GS240(:,2);
VGate240 = GS240(:,3);


tV2402 = GS2402(:,1);
VSwitch2402 = GS2402(:,2);
VGate2402 = GS2402(:,3);


tV2403 = GS2403(:,1);
VSwitch2403 = GS2403(:,2);
VGate2403 = GS2403(:,3);


figure
tiledlayout(2,1)
nexttile
plot(tV240, VSwitch240, 'LineWidth', 2)
xlim([-1.37e-6 6.08e-07])
xlabel('Time [s]')
ylabel('Voltage [V]')
ylim([-70 770])
```

```
hold on
yyaxis right
plot(tV240, VGate240, 'LineWidth', 2)
ylabel('Gate voltage [V]')
legend('Transistor voltage', 'Gate voltage')
ylim([-2 20])
nexttile
plot(tV2403, VSwitch2403, 'LineWidth', 2)
xlabel('Time [s]')
ylabel('Voltage [V]')
legend('Transistor voltage')
xlim([-0.006787 0.006766])


figure
plot(tV240, VSwitch240, 'LineWidth', 2)
title('Second')
% xlim([-1.388e-6 6.11e-07])
xlabel('Time [s]')
ylabel('Switch voltage [V]')
% ylim([-50 700])
hold on
yyaxis right
plot(tV240, VGate240, 'LineWidth', 2)
ylabel('Gate voltage [V]')
% ylim([-5 25])
legend('Switch voltag', 'Gate Voltage')
```

```
%THD analysis 240 Volt
%240 Voltage Class D
Harmmonic = THD240(:,1);
Freuency = THD240(:,2);
rmsvalue = THD240(:,3);
percentvalue = THD240(:,4);


tS240 = VC240(:,1);
tS240B = tS240(1:2000, :);
Vout240 = VC240(:,2);
Vout240B = Vout240(1:2000, :);
Vout240Pos = Vout240(Vout240>0);
VGrid240 = VC240(:,3);
VGrid240B = VGrid240(1:2000, :);
Iout240 = VC240(:,4);
Iout240B = Iout240(1:2000, :);
Igrid240 = -1*VC240(:,5);
Igrid240B = Igrid240(1:2000, :);
Pout240 = -1.*VC240(:,6);


Pgrid240 = -1*VC240(:,7);
```

```
Pgrid240B =Pgrid240(1:2000)';
avgPgrid240B = mean(Pgrid240B,'omitnan')
Vout240average = mean(abs(Vout240), 'omitnan')
Pout240mean = mean(Pout240(1:2000))
Pin240mean = mean(Pgrid240(1:2000))
efficiency = Pout240mean/ Pin240mean*100
IgridRMS = rms(Igrid240B)
ApparentPower = Igrid240B.*VGrid240B;
avgApPower = mean(ApparentPower, 'omitnan')
PF = avgPgrid240B/avgApPower




figure
tiledlayout(2,1)
nexttile
stem(Harmmonic, percentvalue, 'LineWidth', 2)
ylabel('Percent [%]')
xlabel('Number of harmonic')
hold on
stem(Harmmonic, standard2, 'LineWidth',2)
legend('Current measurement', 'Maximum limits for Class C')
nexttile
plot(tS240(1:2000), Pgrid240(1:2000), 'LineWidth', 2)
hold on
plot(tS240(1:2000), Pout240(1:2000), 'LineWidth',2)
xlim([-0.025 0.025])
legend('Input power', 'Output power')
ylabel('Power [W]')
xlabel('Time [s]')







figure
plot(tS240B, VGrid240B, 'LineWidth', 2)
xlim([-0.025 0.025])
hold on
plot(tS240B, Vout240B, 'LineWidth', 2)
ylabel('Grid voltage [V]')
yyaxis right
plot(tS240B, Igrid240B, 'LineWidth', 2)
ylabel('Grid current [A]')
legend('Grid voltage','Output voltage', 'Grid current')


figure
```

```
%230 Voltage at 50Hz
tV230 = GS230(:,1);
VSwitch230 = GS230(:,2);
VGate230 = GS230(:,3);


figure
plot(tV230, VSwitch230, 'LineWidth', 2)
xlim([-1.388e-6 6.11e-07])
xlabel('Time [s]')
ylabel('Switch voltage [V]')
ylim([-50 700])
hold on
yyaxis right
plot(tV230, VGate230, 'LineWidth', 2)
ylabel('Gate voltage [V]')
ylim([-5 25])
legend('Switch voltag', 'Gate Voltage')
```

```
tS230 = VC230(:,1);
Vout230 = -1.*VC230(:,2);
VGrid230 = VC230(:,3);
Iout230 = VC230(:,4);
Igrid230 = -1*VC230(:,5);
Pout230 = -1.*VC230(:,6);
Pgrid230 = -1*VC230(:,7);
Vout230average = mean(abs(Vout230), 'omitnan')


figure
plot(tS230, VGrid230, 'LineWidth', 2)
xlim([-0.025 0.025])
hold on
plot(tS230, abs(Vout230), 'LineWidth', 2)
ylabel('Grid voltage [V]')
yyaxis right
plot(tS230, Igrid230, 'LineWidth', 2)
ylabel('Grid current [A]')
legend('Grid voltage','Output voltage', 'Grid current')
```

```
% 120V at 60Hz
tV120 = GS120(:,1);
VSwitch120 = GS120(:,2);
VGate120 = GS120(:,3);


%120V 60Hz First
tS120 = VC120(:,1);
Vout120 = VC120(:,2);
Pout120 = -1*VC230(:,3);
Igrid120 = -1*VC230(:,4);


 % 120V 60Hz Second
tS1202 = VC1202(:,1);
Vout12022 = VC1202(:,2);
Vgrid1202 = VC1202(:,3);
Iout1202 = VC1202(:,4);
Igrid1202 = VC1202(:,5);
Pout12022 = VC1202(:,6);
Pin12022 = VC1202(:,7);


Vout12022average = mean(abs(Vout12022), 'omitnan')
Pout12022mean = mean(abs(Pout12022), 'omitnan')
Pin12022mean = mean(abs(Pin12022), 'omitnan')
efficiency12022 = Pout12022mean/Pin12022mean*100
Irms12022 = rms(Igrid1202(1:1998))


figure
plot(tS1202, Vgrid1202, 'LineWidth',2)
hold on
plot(tS1202, Vout12022, 'LineWidth',2)
ylabel('Voltage [V]')
yyaxis right
plot(tS1202, Igrid1202, 'LineWidth', 2)
ylim([-0.31 0.31])
ylabel('Ampere [A]')
legend('Grid Voltage', 'Output voltage', 'Grid current')
xlabel('Time [s]')


figure
tiledlayout(2,1)
nexttile
plot(tV120, VSwitch120, "LineWidth",2)
ylabel('Voltage [V]')
xlim([-1.38e-6 6.08e-7])
ylim([-50 500])
hold on
yyaxis right
```

```
plot(tV120, VGate120, "LineWidth",2)
ylim([-2 20])
ylabel('Voltage [V]')
legend('Transistor voltage', 'Gate voltage')
xlabel('Time [s]')
nexttile
plot(tS240(1:2000), Pgrid240(1:2000), 'LineWidth', 2)
hold on
plot(tS240(1:2000), Pout240(1:2000), 'LineWidth',2)
xlim([-0.025 0.025])
legend('Grid power', 'Output power')
ylabel('Power [W]')
xlabel('Time [s]')
```

The second suggested converter

```
% clear
GS120E = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassE\120V
ClassE\ac120classe_oneper4.csv');
GS120E2 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassE\120V
ClassE\ac120classe_oneper7.csv');
THDE120 = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassE\120V ClassE\AC120
ClassE45.csv');


VC120E = readmatrix('C:\Users\k_sta\OneDrive\Documents\M.Sc Electrical
Engineering\Master Thesis\Experimental results\ClassE\120V ClassE\AC120
ClassE48.csv');
standard2 = [nan 2 27 nan 10 nan 7 nan 5 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3
nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan 3 nan]'
```

```
tVC120E = VC120E(:,1);


%THD analysis 240 Volt
%240 Voltage Class D
HarmmonicE = THDE120(:,1);
FreuencyE = THDE120(:,2);
rmsvalueE = THDE120(:,3);
percentvalueE = THDE120(:,4);


tS120E = VC120E(:,1);
Vout120E = VC120E(:,2);
VGrid120E = VC120E(:,3);
```

```
Iout120E = VC120E(:,4);
Igrid120E = -1*VC120E(:,5);
Pout120E = -1.*VC120E(:,6);
Pgrid120E = -1*VC120E(:,7);
Vout120Eaverage = mean(abs(Vout120E), 'omitnan')
Pout120Emean = mean(Pout120E)
Pin120Emean = mean(Pgrid120E)
efficiency = Pout120Emean/ Pin120Emean*100
IgridRMS120E = rms(Igrid120E)


figure
plot(tS120E, VGrid120E, 'LineWidth', 2)
xlabel('Time [s]')
ylabel('Voltage [V]')
hold on
plot(tS120E, Vout120E, 'LineWidth', 2)
yyaxis right
plot(tS120E, Igrid120E, 'LineWidth', 2)
ylabel('Grid current [A]')
legend('Grid voltage', 'Output voltag', 'Grid current')


figure
tiledlayout(2,1)
nexttile
stem(HarmmonicE, percentvalueE, 'LineWidth', 2)
ylabel('Percent [%]')
xlabel('Number of harmonic')
hold on
stem(HarmmonicE, standard2, 'LineWidth',2)
legend('Current measurement', 'Maximum limits for Class C')
nexttile
plot(tS120E, Pgrid120E, 'LineWidth', 2)
hold on
plot(tS120E, Pout120E, 'LineWidth',2)
xlim([-0.025 0.025])
legend('Grid power', 'Output power')
ylabel('Power [W]')
label('Time [s]')
```

```
%120 Voltage at 60Hz
tV120E = GS120E(:,1);
VSwitch120E = GS120E(:,2);
VGate1120E = GS120E(:,3);
VGate2120E = GS120E(:,4);


tV120Ec = GS120E2(:,1);
VSwitch120Ec = GS120E2(:,2);
VGate1120Ec = GS120E2(:,3);
```

```
VGate2120Ec = GS120E2(:,4);


figure
tiledlayout(2,1)
nexttile
plot(tV120Ec, VSwitch120Ec, 'LineWidth', 2)
xlim([-4.999e-4 -4.98e-4])
xlabel('Time [s]')
ylabel('Switch voltage [V]')
legend('Transistor 1 voltage')
% ylim([-50 700])
nexttile
plot(tV120Ec, VGate1120Ec, 'LineWidth', 2)
hold on
plot(tV120Ec, VGate2120Ec, 'LineWidth', 2)
xlim([-4.999e-4 -4.98e-4])
ylabel('Gate voltage [V]')
legend('Gate 1 voltage', 'Gate 2 voltage')
ylim([-5 20])


figure
plot(tV120Ec, VSwitch120Ec, 'LineWidth', 2)
ylabel('Switch voltage [V]')
hold on
yyaxis right
plot(tV120Ec, VGate1120Ec, 'LineWidth', 2)
plot(tV120Ec, VGate2120Ec, 'LineWidth', 2)
legend('Switch voltage', 'Gate voltage 1', 'Gate voltage 2')
ylabel('Gate voltage [V]')
xlim([-4.999e-4 -4.98e-4])
ylim([-5 20])
```