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Designing and Implementation of grid-connected separately excited DC Machine

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Abstract

This thesis presents the design and implementation of SEDC machine which was located at machine laboratory in UiT Narvik campus. To improve the efficiency and to have automatic control, the old passive control needs to be replaced with DC-DC converters based active control method. This thesis explores various DC-DC and grid connected converter with the goal to find a suitable and most efficient for this application. Half bridge VSI was developed and analyses, Filter and PCB for the Three-phase VSI was developed.

Preface

This thesis is submitted in partial fulfillment of the requirement for the Master of Science (MSc) in Electrical Engineering at The Arctic University of Norway (UiT). I am grateful to my supervisor Umer Sohail, PhD Candidate for advice and support. I am so much grateful for his ultimate support towards the completion of the thesis. I am also grateful to all the teaching and non-teaching staff of the Department of Electrical Engineering at UiT especially Trond Østrem, Associate Professor and Ketil Hansen, Chief Engineer Electronics Laboratory for the opportunity they give me to improve my knowledge in electrical engineering.

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Nomenclature and notation

Abbreviations

AC	Alternating current
DC	Direct current
SEDC	Separately excited direct current.
VSC	Voltage source converter
HB	Half bridge
DAB	Dual active bride
DHB	Dual half bridge
IBDC	Isolated bidirectional direct current
NIBDC	Non-isolated bidirectional direct current
MOSFET	Metal-oxide-semiconductor-field-effect transistor
EMF	Electromagnetic force
VOC	Voltage oriented control
THD	Third harmonics distortion
PCB	Printed circuit board.
SVM	Space vector modulation
SPWM	Sinusoidal Pulse Width modulation
IGBT	Insulated Gate Bipolar Transistor
VSI	Voltage source inverter
PLL	Phase-locked loop

Symbols

V_{grid}	Grid voltage
V_{dc}	DC-link voltage
i_{dc}	DC current
L_c	Converter side inductor

L_s, L_{grid}	Grid side inductances
L	inductor
C	Capacitor
V	Voltage
I	Current
I_w, I_f	Excitation current
V_w, V_f	Excitation voltage
R_a	Armature Resistance
L_a	Armature inductance.
R_f	Field resistance
L_f	field inductance
E_g	Back Emf
B	Viscous friction constant
TL	Load torque
J	Inertia
Sw	Switch
V_{ref}	Reference voltage
V_c	Carrier voltage
m_a, m_i	Modulation index
R_d	damping resistance
P_{dc}	DC-link power
P_{ac}	Instantaneous AC power
f_{sw}	Switching frequency
f_g	Grid frequency.

1 Introduction

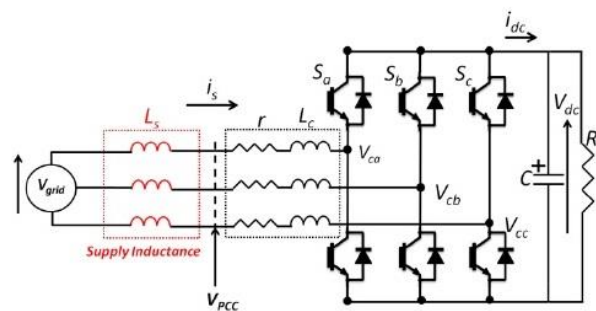
This chapter describes the overall overview of the whole project, objectives, limitations, and thesis outline.

1.1 Background

Controlling the separately excited DC (SEDC) machine is essential because it helps regulate the motor's speed, torque, and direction of rotation. Without proper control, the motor may not operate as desired and at the moment the SEDC machine in our laboratory is being controlled by variable rheostat and all the machines (count the number) are getting the power from thyristor based central rectifier, which has stability issues. To improve the efficiency and to have automatic control, there is need to develop DC-DC converters based active control method. The SEDC machines could be able to run in both generator and motor mode, so the converter system should be bi-directional. The machines have separate field and armature circuits, and hence, speed and torque control are easy [1]. A picture of SEDC machine present at our laboratory and Two level grid connected converter [2] are shown in Figure 1.0.



(a)



(b)

Figure 1.0: SEDC Machine (b) Two level three phase grid connected rectifier [2].

1.2 Presentation of the whole project

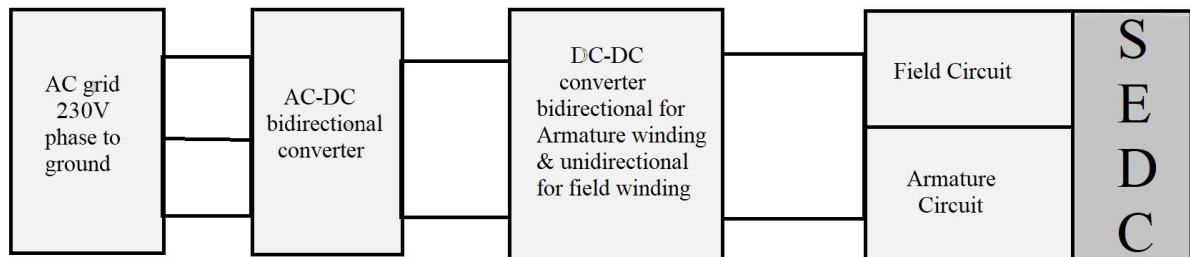


Figure 1.1: System diagram

As shown in Figure 1.1 above, the whole system was presented. The overall DC machine control system is separated into two parts. The first part is a rectifier which is electronically controlled, and which converts the AC power to DC power which I focus throughout this thesis. The second part is a DC-DC converter also electronically controlled and which we already have.

The two converters (Rectifier and DC-DC converter) mentioned earlier must therefore also be able to operate in two different modes. If the DC machine operates in motor mode, then it consumes power which is sent from the electrical grid. If the DC machine operates in generator mode, then it is the machine that creates power and sends it to the electrical grid [3].

The control signal changes for the rectifier circuit to make it operate as an inverter. However, the control of the DC-DC converter changes depending on the mode. If the DC machine operates in motor mode, then the DC-DC converter connected to Armature winding will operate as a voltage step-down device called a Buck converter. However, if it works in generator mode then the converter will work as a voltage booster called Boost Converter.

1.3 Objectives

The primary objectives of this thesis are:

1. Study about working of SEDC machines and voltage source rectifiers
2. Hardware implementation of rectifier
3. Analysis of result.

1.4 Limitations

All simulation and analysis are limited to Half bridge rectifier. Therefore, it should be done for three-phase rectifier.

1.5 Outline of the thesis

The report consists of 6 chapters.

- Chapter 1 shortly describes the overall overview of the whole model, objectives, limitations, contributions and thesis outline.
- Chapter 2 cover literature review about SEDC machines and DC-DC converter.
- Chapter 3 outline literature review on Voltage source converter.
- Chapter 4 describes hardware implementation of Half bridge voltage source converter.
- Chapter 5 describes Experimental verification, control signal generation in dSPACE and describe how the output was improved.
- Chapter 6 outline Three-phase converter design from the previous research was improved by designing a LCL filter. In addition, it's also outline how the PCB was design.
- Chapter 6 describes analysis on Half bridge AC-DC converter.
- Chapter 7 gives a short conclusion of the thesis. It also gives suggestions for further work.

2 Literature review on SEDC Machines and DC-DC Converters

This chapter describe the literature review of the previous works on SEDC machines and DC-DC converter.

2.1 SEDC Machine

A separately excited DC machine is a type of DC motor where the field winding is not connected to the armature winding. Instead, the field winding is supplied with a separate DC voltage source. Like other motors, these devices also have both rotors and stators. Stator refers to the static section of the device, which contains the field windings. The rotor is the rotating armature which consists of armature coils or windings [4].

Advantages

- control simplicity.
- good dynamic properties.

Disadvantages:

- complex construction.
- high cost.
- low reliability.
- poor weight to power ratio.
- can't work in potentially explosive environment.
- produces electromagnetic interference.

2.1.1 Working principles of SEDC motor

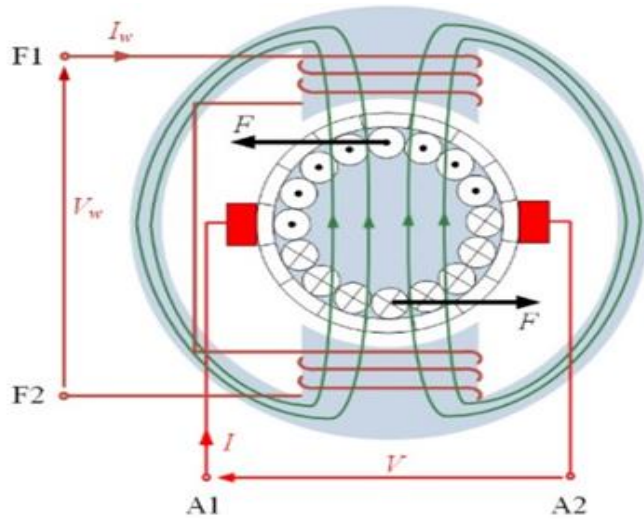


Figure 2.0: Separately excited dc motor [5]

As shown in Figure 2.0, The excitation winding is powered by a DC voltage V_w . The excitation current I_w in that winding produces a magnetic field that penetrates the armature. The armature winding is powered by DC voltage V via a commutator and brushes, which causes the flow of current I . As a result of the magnetic field and the current, a force is acting on the armature, which starts rotating. The purpose of the commutator is to ensure the current flow through the relevant parts of the armature windings, so that the force acting on the armature is maximum [5].

2.1.2 Mathematical model of SEDC

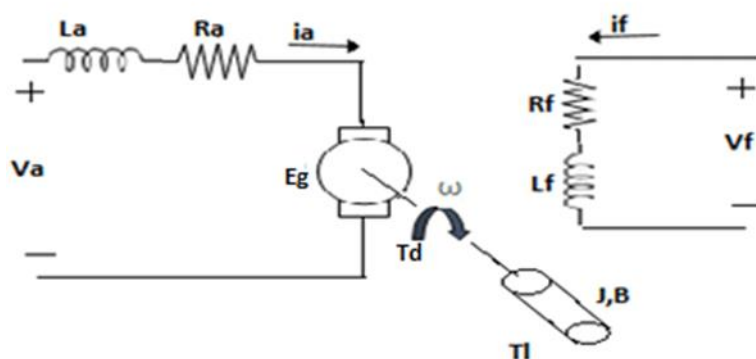


Figure 2.1: Circuit Diagram of a Separately Excited DC Motor [6].

FIELD AND ARMATURE EQUATION:

Field voltage is given by:

$$V_f = R_f i_f + L_f * \frac{di_f}{dt} \quad (2.1)$$

where i_f , R_f and L_f are the field current, field resistance and field inductance respectively.

Armature voltage is given by:

$$V_a = R_a i_a + L_a * \frac{di_a}{dt} + E_g \quad (2.2)$$

where i_a , R_a and L_a are the armature current, armature resistance and armature inductance respectively.

The motor back emf, is expressed as

$$E_g = K_v \omega i_f \quad (2.3)$$

where K_v is the motor voltage constant (in V/A-rad/sec) and ω is the motor speed (in rad/sec)[6]

TORQUE EQUATION AND ANALYSIS

For normal operation, the developed torque must be equal to the load torque plus the friction and inertia, i.e. :

$$T_d = J * \frac{d\omega}{dt} + B\omega + T_l \quad (2.4)$$

Where,

B: Viscous friction constant (N.m/rad/sec)

T_l : Load Torque (N.m)

J : Inertia of the motor (Kg.m²)

Developed Torque is also expressed as:

$$T_d = K_t i_f i_a \quad (2.5)$$

Where,

K_t : Torque constant [6]

When the excitation winding is supplied with a constant value of voltage, the flux linkage and field current are also constant. For constant flux linkage the linear model of the motor applies.

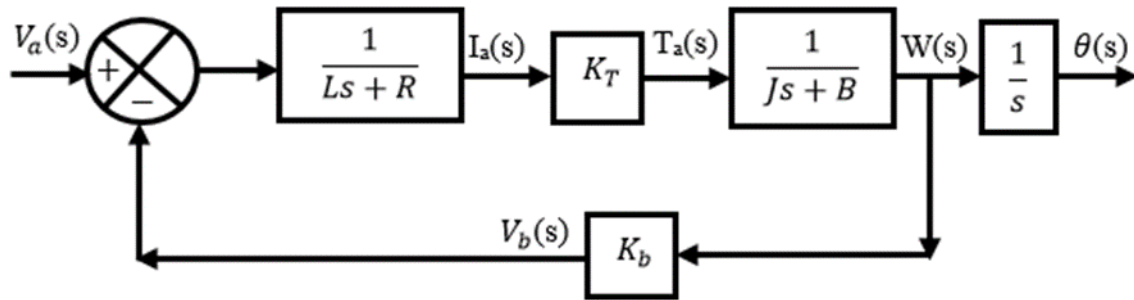


Figure 2.2: Mathematical Model of separately excited DC Motor [7].

As shown in Figure 3.0, a block diagram for the linear model was presented.

2.1.3 Motor Parameters

The DC motor parameters used in this thesis are calculated using lock rotor test from the previous research [8] :

Field Circuit :

- $R_f = 168$ (2.6)

- $L_f = 36.43$ H (2.7)

Armature Circuit :

- $R_a = 2.03$ (2.8)

- $L_a = 0.126$ H (2.9)

Inertia Moment :

- $J = 0.457$ kg.m² (2.91)

2.2 DC-DC converters

A device or circuit known as a DC-DC converter can change the polarity of a DC voltage while converting it from one level to another. Applications for DC-DC converters include electric vehicles, solar power systems, and portable gadgets.

2.2.1 Bidirectional DC-DC Converter

A bidirectional DC-DC converter has a significant role in power electronics. They cover the requirement for power connection from the source to the load. The bidirectional DC-DC converter is used to capture the kinetic energy of the motor and charge the battery through regenerative braking . It is also used to smooth the power flow to the grid and provide power conditioning. which will improve the quality of the power delivered to the load and increase the efficiency of the charging system [9].

The device has switch on and off capabilities at high frequencies, for example, in a Dual Active Bridge (DAB) and isolated bidirectional DC-DC converter that will provide both savings of the surplus energy, galvanic isolation, and efficient power flow without wasting the energy[10].

To control the charging and discharging of the battery storage system, it is necessary to use a bidirectional DC-DC controller. By choosing a modern converter that has the possibility of operating between two fixed voltages, the battery storage system voltage and the DC bus voltage. A bidirectional DC-DC converter is implemented with two PI controllers with two different value of the gain, one value for the charging process and other value for the discharging process to achieve the desired reference current signal[10].

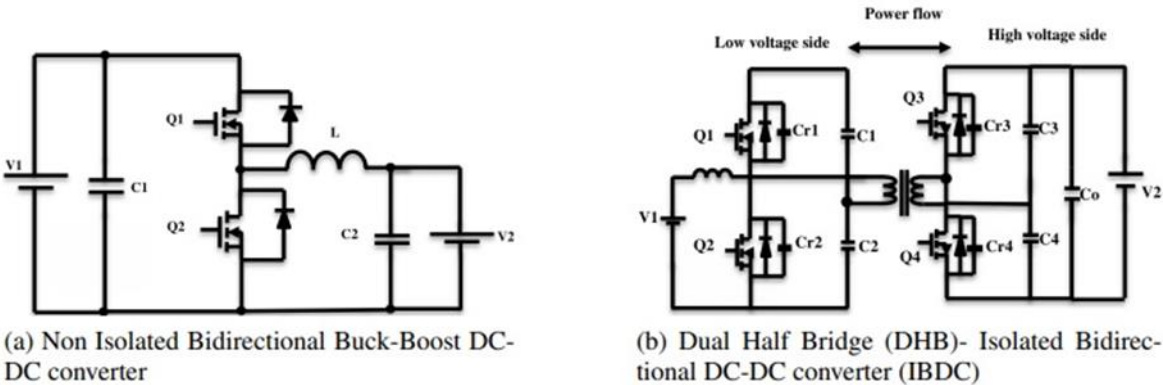


Figure 2.3: Bidirectional DC-DC converter [10].

The bidirectional DC-DC converters are classified into two types as shown in Figure 2.3

- Non-Isolated Bidirectional DC-DC Converter (NIBDC).
- Isolated DC-DC Converter (IBDC).

2.2.2 Non-Isolated Bidirectional DC-DC converter (NIBDC)

The non-isolated bidirectional DC-DC converter can provide electrical isolation between source and load without using a high-frequency transformer. Due to safety reasons, these are not recommended for use in high-power applications. The advantages of this type of converter are that it is easy to control, simple to design, and has a low weight because it does not use a transformer. Example of this converters are Bidirectional Buck-Boost converter, Bidirectional CUK converter, Cascaded Bidirectional Buck-Boost converter, Half-bridge bidirectional converter, etc [10].

Bidirectional Buck-Boost converter has been used in grid-connected applications because the topology is simple and have high efficiency. As shown in Figure 2.3a, it has two switches, and those are operating in anti-parallel according to the duty cycle. The circuit consists of the combination of buck-boost converters. Q1 is conducting during the boost mode, and Q2 is not connected. The opposite, when Q2 is active than Q1 will not conduct [10].

2.2.3 Isolated DC-DC Converter (IBDC)

There are many topologies of isolated converters, among those are Dual Half Bridge IBDC and Dual Active Full Bridge IBDC. How IBDC work is by using a high-frequency transformer to ensure galvanic isolation. It is primarily to have the galvanic isolation to avoid the overload condition for EMV. Another benefit of galvanic isolation is to reduce the noise and for voltage matching between different conditions. This type of converters has two stages, and those stages connected through a high-frequency transformer, the first stage is DC-AC and second stage is AC-DC. Dual Active Full Bridge IBDC are more suitable choice, use in hybrid energy system and will not be further considered for this thesis application. Dual Half Bridge IBDC in Figure 2.3b have also been used in grid applications [10].

However, Isolated DC-DC converter will provide the safety standard of galvanic isolation. Dual half bridge IBDC is an excellent converter to implement in EMV, include with their high power density, soft switching technique, and simple control technique. However, it also has a disadvantage, which is heavy because of the transformers [10].

In this thesis, the two dc-dc converters used are:

- Unidirectional chopper for the field circuit
- Bidirectional (full bridge) for the armature circuit

Unidirectional chopper for the field circuit

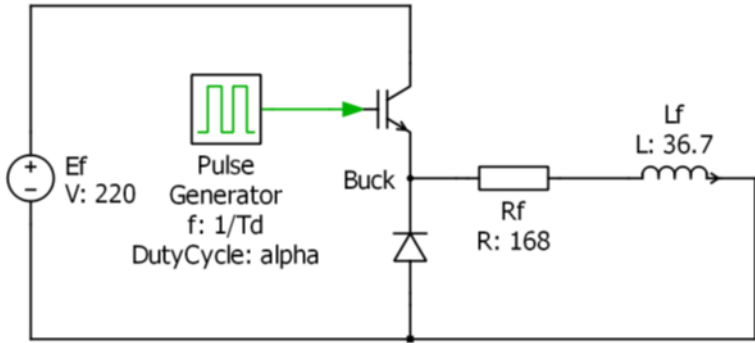


Figure 2.4: Field Circuit with Unidirectional Chopper [11].

The chopper used in Figure 2.4 is a BUCK converter. It allows to control the field circuit of the DC motor, thus enabling the control of the induction field. The Buck converter is supplied with a 220V DC voltage so that the average output voltage could reach between 0V to 220V. However, it is obvious that we need to keep a minimal voltage value to run the motor. To ensure that the output voltage follows a given reference, we must use the duty cycle as a control. The average model of the converter highlights the linear relationship between the output voltage and the duty cycle for a constant supply voltage [11].

Bidirectional (full bridge) for the armature circuit

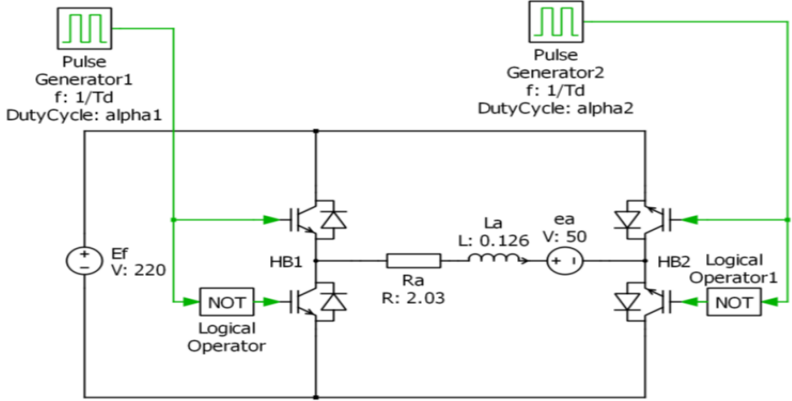


Figure 2.5: Armature Circuit with Full Bridge [11].

The H-Bridge is a classic converter used here to operate the motor in the 4 quadrants. Indeed, the motor could be run as a generator or a motor so the output current could be positive or negative (positive or negative torque) and the motor can have a positive or a negative speed ensuring that the back-EMF can be positive or negative. Therefore, it is necessary to build a converter which allows a positive and negative output voltage and current. The H-Bridge converter is a classic application for such systems.[11]

2.2.4 DC-DC control algorithms

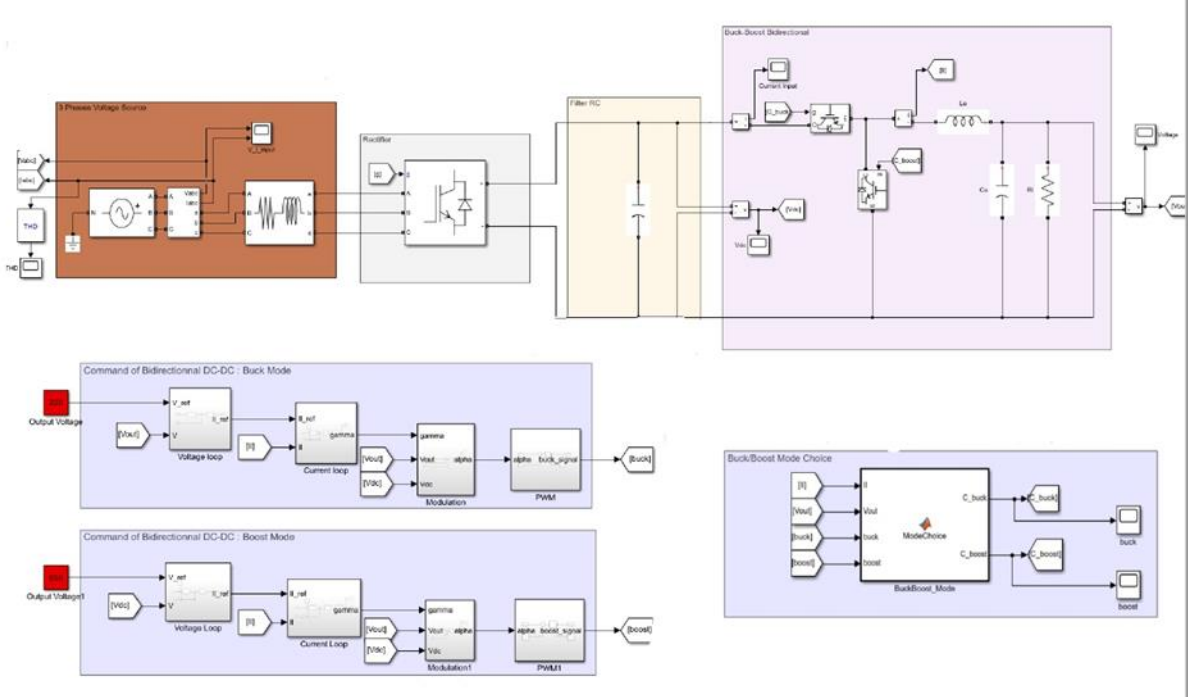


Figure 2.6: Simulink model of the control model for the DC-DC converter[12].

The control system shows in Figure 2.6 was design and simulated from the previous research [12] on this project. The design of this system allows to supply the DC motor with a controlled 220V DC and to control the current input.

3 Literature review on Voltage Source Converters

This chapter present the literature review about voltage source converter.

3.1 Voltage source converter

The Converter used in this project is bidirectional AC-DC converter which convert alternating current (AC) power to direct current (DC) power in one direction and then convert DC power back to AC power in the opposite direction. This type of converter is used in applications where power needs to flow bi-directionally.

3.2 AC-DC bidirectional converter topologies

Different converter topologies result different levels of quality and complexity. Therefore, the selection of a suitable topology almost depends on the nature and the requirements of the application.

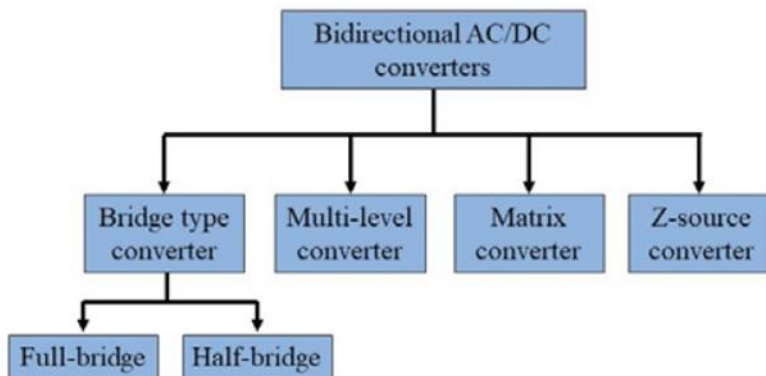


Figure 3.0 A basic classification of AC/DC bidirectional converter topologies [13].

various converter topologies for bidirectional converters can be found in literature [13].

Bridge type converter was choosing for this thesis for the following:

- High voltage capability: Bridge converters can handle high input voltages, making them suitable for use in applications where input voltages are much higher than the nominal output voltage.
- Low output ripple: Bridge converters produce low output ripple, which reduces the need for additional filtering components.
- Wide input voltage range: Bridge converters can operate over a wide input voltage range, making them suitable for use with a variety of input sources.

- Simple design: Bridge converters are easy to design and require only a few external components, making them cost-effective and easy to manufacture.
- High efficiency: Bridge converters are highly efficient and can achieve efficiencies of up to 95%, which reduces power losses and improves overall system performance.
- High power density: Bridge converters are compact and lightweight, making them suitable for use in high-power applications where space is limited.

3.3 Full Bridge Bidirectional Converter

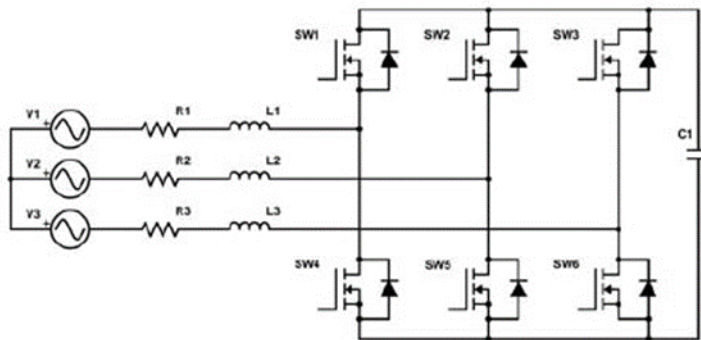


Figure 3.1: Voltage source – full bridge bidirectional converter [13].

Figure 3.1 shows the schematic diagram of voltage source converter, there six fully controlled switches SW1, SW2, SW3, SW4, SW5 and SW6 in which each two MOSFETs are connected with each phase of source. The MOSFETs connected in one leg does not turn on at time if we do so there is short circuit occur between the upper and lower MOSFET.

The most basic AC/DC topology that has bidirectional conversion capability is the bridge type voltage source converter (VSC). There are two bridge type configurations, half-bridge and full bridge. Figure 3.1 shows the full bridge converter configuration. Inverting mode of both bridge converters use control inputs for switching; but number of control inputs are higher for full-bridge converter compared to half-bridge. This makes the controller more complex and costly. Although half-bridge is much simpler and cheaper topology, it generates a high harmonic content, so requires a large harmonic filter [13].

Moreover, the voltage stress on components is lower in full-bridge and can use low rated switches which reduces the cost. Generally, the two level VSC is used to interface with low voltage grid network (< 500 V). VSC operates in buck mode (step-down) during dc-to-ac power conversion (inverter) and in boost mode (step-up) in ac-to-dc conversion (rectifier).

This necessitates a two-stage configuration with an additional structure to control the voltage to match the desired AC output with the grid and DC output with the battery for inverter and rectifier modes respectively [13].

Full-bridge AC/DC converter coupled with a buck-boost converter is a quite general converter structure in bidirectional on-board EV chargers [14]. Further, VSC topology is utilized in many inductive power transfer designs to rectify low frequency grid voltage for high frequency conversion stage.

3.4 Analytical Modeling

In the design of control systems for PWM converters, analytical models are important tools for predicting dynamic performance and stability limits of different control laws and system parameters [15].

3.4.1 State Space Modeling of Grid Connected VSC

The system to be modeled is described in figure 3.2, the inductance L_{grid} is assumed to be zero and the q-axis of the dq-frame is synchronized to the vector set up by the voltage u_{2a}, u_{2b}, u_{2c} . If a significant inductance present, the angle of the dq-frame changes rapidly at steps in the line currents, and the inductance L_{grid} should be included in the analytical models [15].

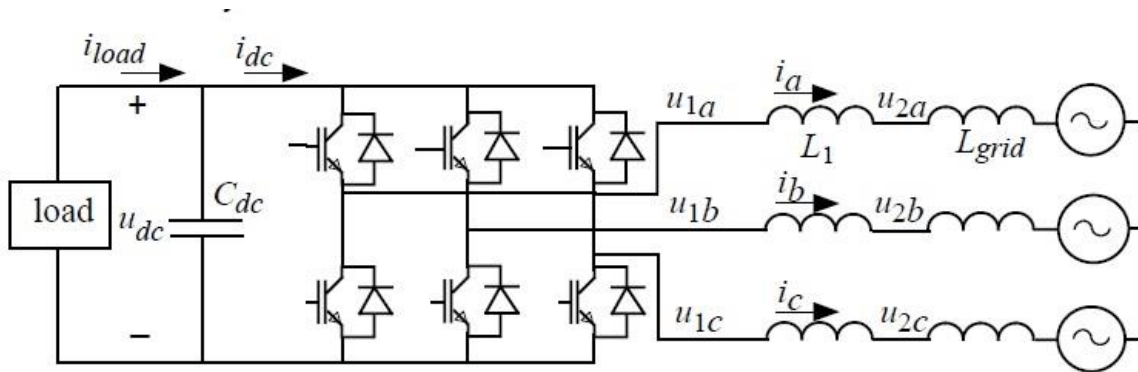


Figure 3.2: Grid connected VSC [15]

The ac side of the converter system is modeled by differential equations for each phase. Assuming that the inductors are not saturated and that iron losses and copper losses due to the skin effect can be neglected, the equations for the l-filter are.

$$L_1 \frac{di_a}{dt} + R_1 i_a = u_{1a} - u_{2a} \quad (3.1)$$

$$L_1 \frac{di_b}{dt} + R_1 i_b = u_{1b} - u_{2b} \quad (3.2)$$

$$L_1 \frac{di_c}{dt} + R_1 i_c = u_{1c} - u_{2c} \quad (3.3)$$

By using vector notation, these equations can be written in $\alpha\beta$ – frame

$$L_1 \frac{d\underline{i}^{\alpha\beta}}{dt} + R_1 \underline{i}^{\alpha\beta} = \underline{u}_1^{\alpha\beta} - \underline{u}_2^{\alpha\beta} \quad (3.4)$$

And in the rotating dq – frame as

$$L_1 \frac{d\underline{i}^{dq}}{dt} + (R_1 + j\omega_g L_1) \underline{i}^{dq} = \underline{u}_1^{dq} - \underline{u}_2^{dq} \quad (3.5)$$

The decoupled equation can be written in the state space form as

$$\frac{dx_L}{dt} = A_L x_L + B_L u_L \quad (3.6)$$

Where the state vector and the input vector are defined by

$$x_L = [i_d \quad i_q]^T \quad (3.7)$$

And

$$u_L = [u_{1d} \quad u_{1q} \quad u_{2d} \quad u_{2q}]^T \quad (3.8)$$

respectively. The system matrix and the input matrix are giving by

$$A_L = \begin{bmatrix} -\frac{R_1}{L_1} & \omega_g \\ \omega_g & -\frac{R_1}{L_1} \end{bmatrix} \quad (3.9)$$

And

$$B_L = \begin{bmatrix} \frac{1}{L_1} & 0 & \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \end{bmatrix} \quad (3.10)$$

The state space equation for the ac side of the system is linear for the L-filter.

The dc side side of the system is modeled by the equation

$$C_{dc} \frac{du_{dc}}{dt} = i_{load} - i_{dc} \quad (3.11)$$

The current in the dc link can be found from the power of the ac side since the power on the dc side must be equal to the power on the ac side of the converter. Here, the losses in the valves are neglected. The instantaneous power on the ac side and the side of the converter can be obtained from

$$p_{ac} = \text{Re} \left\{ \underline{u}_1^{\alpha\beta} \underline{i}_1^{\alpha\beta*} \right\} \quad (3.12)$$

And

$$p_{dc} = u_{dc} i_{dc} \quad [15] \quad (3.13)$$

3.5 Pulse width modulation (PWM)

Switched converters are more efficient than linear regulators, since transistors only are operated in fully open or closed position. To generate those switching signals, different types of switching and modulation techniques are applied such as:

- Sinusoidal PWM(SPWM)
- Space vector PWM(SVPWM)

3.5.1 Sinusoidal PWM(SPWM)

Sinusoidal PWM is a typical PWM technique. In this technique, the sinusoidal AC reference voltage (V_{ref}) is compared with the high-frequency triangular carrier wave (V_c) in real time to determine switching states for each pole in the inverter [16]. As shown in Figure 3.3 After comparing, the switching states for each pole can be determined based on the following rule:

- Voltage reference (V_{ref}) > Triangular carrier (V_c): upper switch is turned on (pole voltage = $V_{dc}/2$)
- Voltage reference (V_{ref}) < Triangular carrier (V_c): lower switch is turned on (pole voltage = $-V_{dc}/2$)

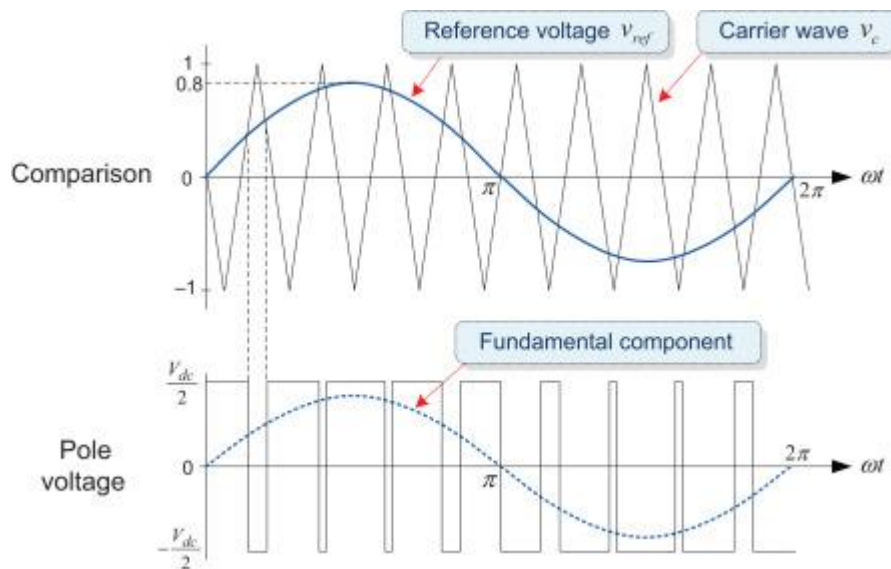


Figure 3.3: Sinusoidal PWM technique [16].

The magnitude of the modulated signal varies in a sinusoidal manner. During half cycle, it has many pulses with their ON time increasing gradually and it again starts decreasing after half cycle.

The modulation index (m_i) controls the harmonic content of the output voltage waveform and also it is directly proportional to the magnitude of the fundamental component of the output.

$$m_i = \frac{V_{ref}}{V_c} \quad (3.14)$$

3.5.2 Space Vector PWM(SVPWM)

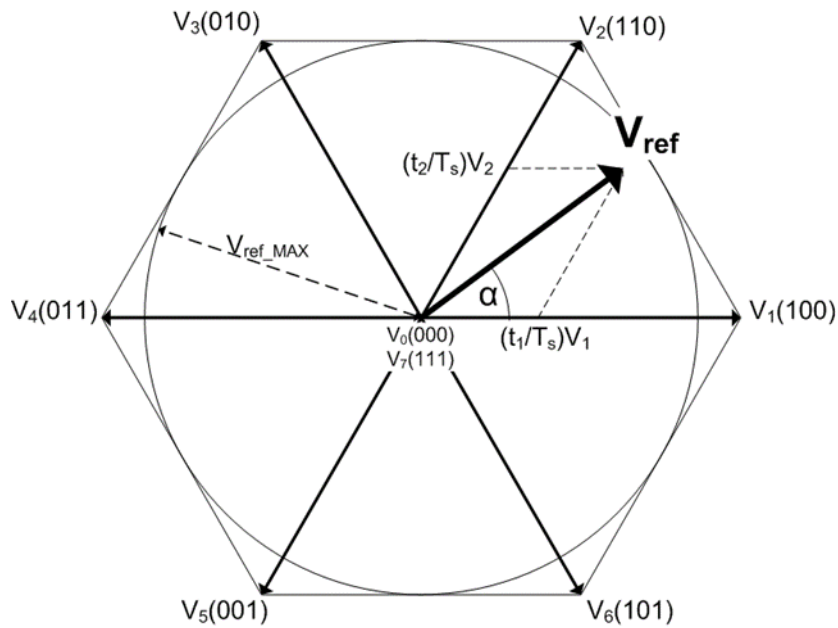


Figure 3.4: All eight possible switching vectors for a three-leg inverter using space vector modulation [17]

Figure 3.4 above represent possible output combination of the switches. The vectors are defined in such away that $V_1(100)$ shows first leg is ON while the others are OFF, this also applied for the rest of the vectors represent in the figure. In addition there are also two zero state (000) and (111) which present the three phase short circuit of the output.

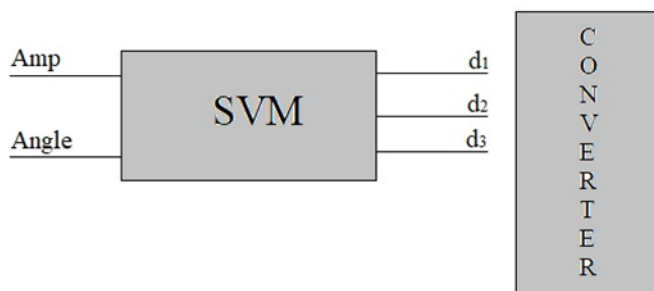


Figure3.5 : block diagram of space vector modulation

Figure 3.5 shown the block diagram of space vector modulation, Where (d_1, d_2, d_3) are controlling upper mosfet while $(\bar{d}_1, \bar{d}_2, \bar{d}_3)$ controls the lower mosfet of the converter.

Maximum linear Amplitude

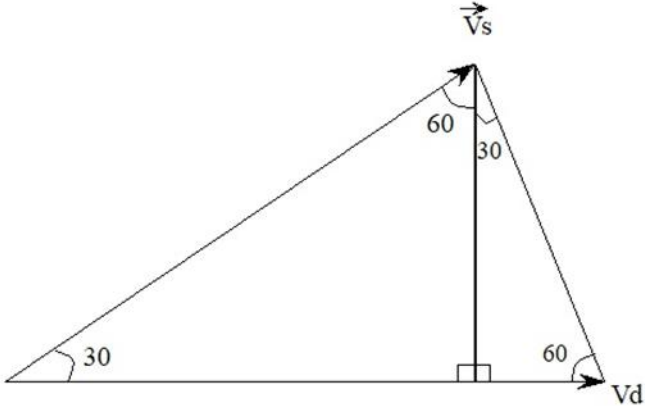


Figure 3.6: Mathematical relationship between V_s and V_d.

$$\vec{V}_s = \cos 30^\circ * V_d = \frac{\sqrt{3}}{2} V_d \approx 0.866 * V_d \tag{3.15}$$

0.866 is very important in design of control system because the lower it get the higher dc link voltage is needed to produce the required reference linear voltage. Therefore, SVM required less dc link voltage than other type of modulations.

Switching Times

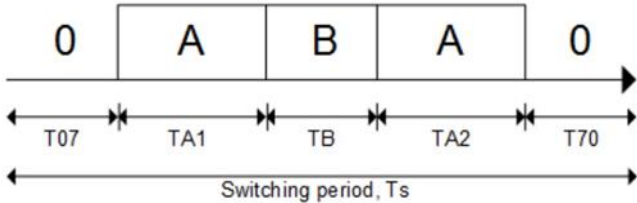


Figure 3.7: Switching times for SVM.

Switching times are presented in Figure 3.6, for modulation of a certain output voltage of the converter \vec{V}_s . In this strategy, A is one vector and B is another vector. They are active for the

time TA and TB. In addition, there are two zero vectors where all upper or lower transistors are closed, (000) and (111).

With respect to Figure 8

$$\frac{\sin\left(\frac{\pi}{3}-\alpha\right)}{a} = \frac{\sin\left(\frac{2\pi}{3}\right)}{|\vec{V}_s|} = \frac{\sqrt{3}}{|\vec{V}_s|} \Rightarrow a = \frac{2}{\sqrt{3}}|\vec{V}_s| \cdot \sin\left(\frac{\pi}{3}-\alpha\right) \quad (3.16)$$

$$\frac{\sin(\alpha)}{b} = \frac{\sqrt{3}}{|\vec{V}_s|} \Rightarrow b = a = \frac{2}{\sqrt{3}}|\vec{V}_s| \cdot \sin(\alpha) \quad (3.17)$$

$$a = \frac{t_1}{T_s} V_1, \quad b = \frac{t_2}{T_s} V_2, \quad |V_1| = |V_2| = V_d \quad (3.18)$$

$$t_1 = \frac{2}{\sqrt{3}} \frac{|\vec{V}_s|}{V_d} T_s \cdot \sin\left(\frac{\pi}{3}-\alpha\right), \quad t_2 = \frac{2}{\sqrt{3}} \frac{|\vec{V}_s|}{V_d} T_s \cdot \sin(\alpha) \quad (3.19)$$

$$D_A = \frac{t_1+t_2}{T_s} = \frac{2}{\sqrt{3}} \frac{|\vec{V}_s|}{V_d} \left(\sin\left(\frac{\pi}{3}-\alpha\right) + \sin(\alpha) \right) \quad (3.20)$$

$$D_B = \frac{t_2}{T_s} = \frac{2}{\sqrt{3}} \frac{|\vec{V}_s|}{V_d} \cdot \sin(\alpha) \quad (3.21)$$

$Valid : 0 \leq \alpha \leq \frac{\pi}{6}$

3.6 Gate driver Circuit

A MOSFET gate driver circuit is a circuit used to drive the gate of a MOSFET, which is typically used as a power switch in electronic circuits. The gate driver circuit is used to control the turn-on and turn-off of the MOSFET, and to ensure that the MOSFET operates in an efficient and reliable manner.

Since the voltage from the micro controller is significantly low to operate the MOSFET, so its necessary to connect the gate driver circuit to amplify the voltage so that fast switching is achieved.

As shown in previous sections, power MOSFETs present excellent characteristics and performances to be implemented in power converters. However, fast switching in high voltage applications may cause considerable surge voltages, spike currents, high-frequency leakage currents, and various electromagnetic interference (EMI) issues, due to high dv/dt and/or di/dt . To address these issues, the gate drive circuit must be optimized to achieve the best performance from the power semiconductor device [18]

There are different topologies in gate driver circuit such as:

- Elementary MOSFET drive circuit.
- Double emitter-follower drive circuit.
- IC drive with double emitter-follower buffer.

3.7 Deadtime

Dead time in a voltage source inverter refers to a time period during which both the high-side and low-side switches of a given phase are turned off to prevent them from conducting simultaneously, which would cause a short-circuit and damage the inverter. This dead time is typically implemented in the control system of the inverter and can be adjusted to optimize the system's performance. The duration of the dead time should be long enough to ensure that the switches are turned off before their respective counterparts are turned on, but not so long that it negatively impacts system efficiency and/or introduces distortion into the inverter output waveform.

In Voltage Source Inverters (VSI), dead time refers to the time duration in which both the upper and lower switching devices (normally IGBTs or MOSFETs) are off to prevent shoot-through currents. During dead time, there is no voltage output from the VSI.

The dead time is typically implemented using driver circuits that control the switching devices. The purpose of dead time is to allow the current to flow through the load during the switching transitions between upper and lower devices, which prevents short-circuits and damage to the switching devices. The dead time in a VSI can be adjusted by changing the duration of the off period for both the upper and lower switching devices. The optimal level of dead time depends on the specific application and must be chosen carefully to balance the trade-off between switching losses and short-circuit protection.

3.8 Control algorithms for voltage source converter

Control algorithms for voltage source converters have developed from analog circuits to software in modern microcontrollers and digital signal processors (DSP). Algorithms originally made for analog circuits have in many case continued in digital form, while the digital revolution has resulted in algorithms utilizing the new possibilities. Over the years, a whole range of control algorithms has been proposed [19].

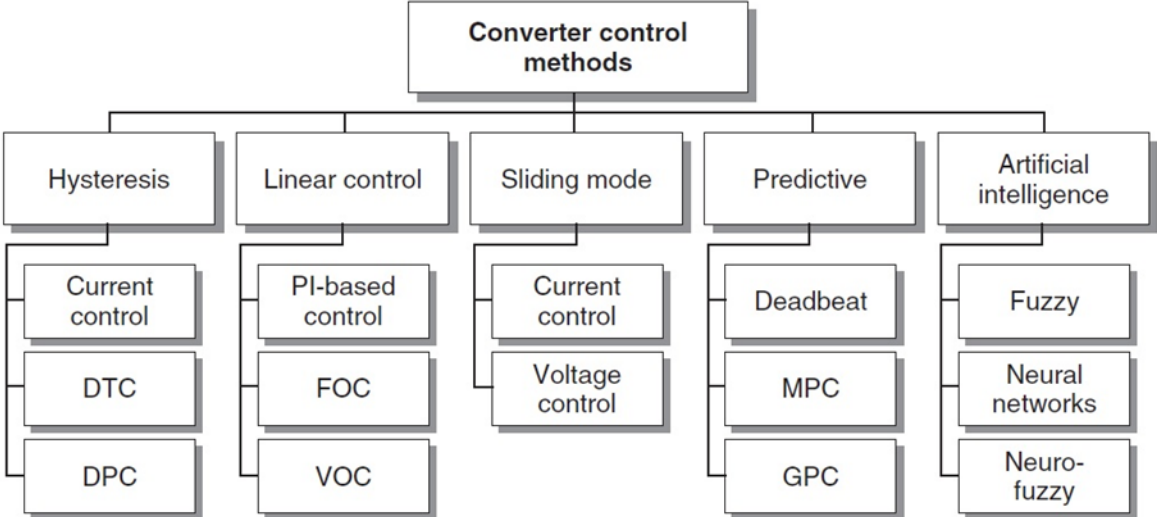


Figure 3.8: Different types of converter control schemes for power converters and drives (GPC Generalized Predictive Control)[20].

One of the most common control methods for voltage source converter(VSC) is the linear control, which is used in combination with a modulator. For grid connected converters, voltage oriented control (VOC) has been a common choice, both in synchronously rotating and stationary reference frame[21].

A detail review of the different control algorithms in figure 3.8 is well describe in the literature review and is out of this thesis. In order to implement VOC, the grid voltage angle has to be known for the Park transformation. This is commonly achieved by using a phase locked loop (PLL) [20].

The control system used in this converter was already designed and simulated by a former internship student, Marion Ribout [12]. The system control scheme is as follows.

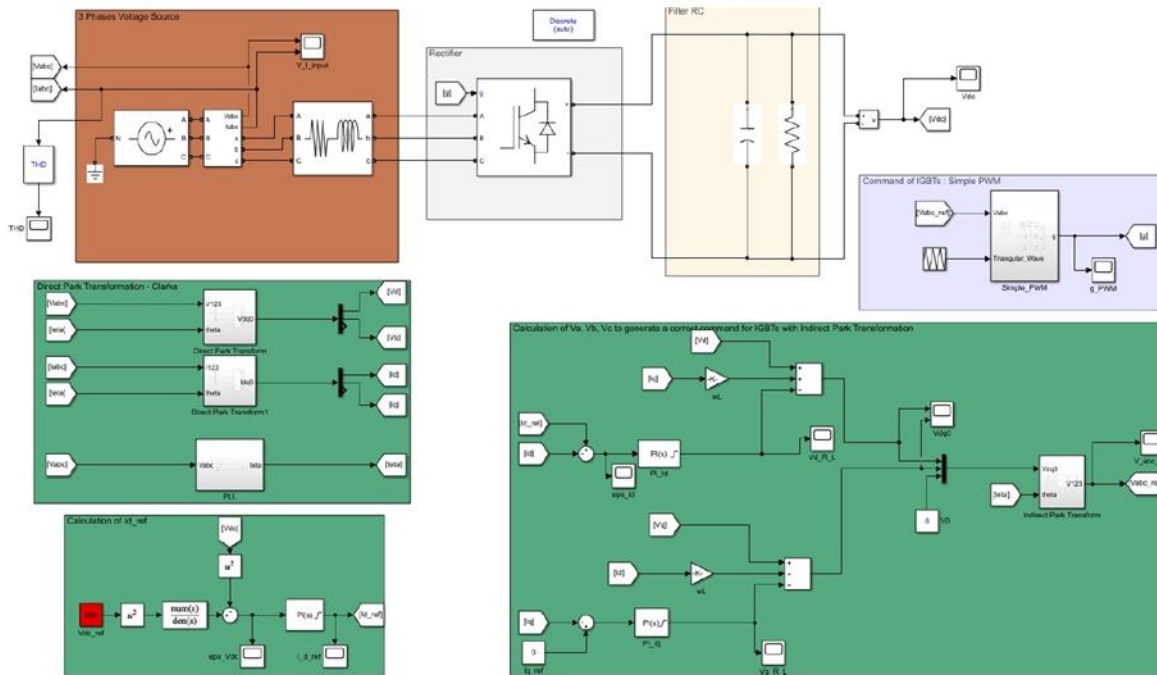


Figure 3.9 : Simulink model of the control system for Voltage source converter[12].

In Figure 3.9, This system makes it possible to control the output voltage of the rectifier. For that, we set a reference value (V_{dc_ref}), and its goal is to maintain this value in output. In this case, the setpoint chosen is 650 volts.

3.9 Filter design

Filter is an essential part of a grid connected converter, since the pulse width modulated voltages |needs to be filtered in order to inject a sinusoidal current to the grid. There are several filter types, but three common ones are:

- L-filter
- LCL-filter
- LC-filter

Due to the more compact design and better attenuation, LCL filter is preferred over L-filter in modern converters.

3.9.1 LC-filter design

Inductor design:

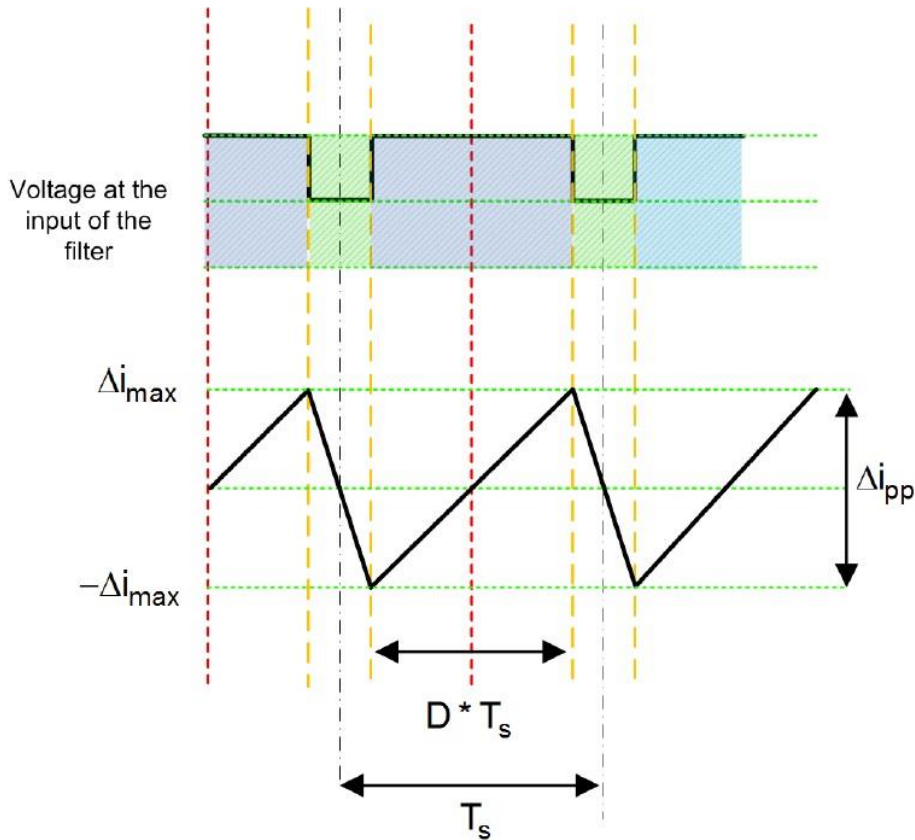


Figure 3.10: Current ripple calculation [22].

In Figure 3.10 above, shows the voltage and current ripples before filter.

The voltage across the inductor is given by:

$$V_L = L_i \frac{di}{dt} \quad (3.22)$$

For the full-bridge inverter with an AC output, write the equation as:

$$\Rightarrow (V_{Bus} - V_o) = L_i * \frac{\Delta i_{pp}}{DT_s} \quad (3.23)$$

Where $T_s = \frac{1}{F_{sw}}$ is the switching period. Now, rearrange the current ripple at any instant in the

AC waveform, giving as:

$$\Rightarrow \Delta i_{pp} = \frac{D * T_s * (V_{bus} - V_o)}{L_i} \quad (3.24)$$

Assuming the modulation index to be m_a , the duty cycle is giving as:

$$D(\omega t) = m_a * \sin(\omega t) \quad (3.25)$$

The output of the inverter must match the AC voltage as it is safe to assume:

$$V_o = V_{DC} * D \quad (3.26)$$

Therefore,

$$\Delta i_{pp} = \frac{V_{Bus} * T_s * m_a * \sin(\omega t) * (1 - m_a \sin(\omega t))}{L_i} \quad (3.27)$$

As seen in Equation (3.27), the peak ripple is a factor of where the inverter is in the sinusoidal waveform (for example, the modulation index). To find the modulation index where the maximum ripple is present, differentiate Equation (3.27) with regards to time to get Equation (3.28), and equate to zero.

$$\frac{d(\Delta i_{pp})}{dt} = K \{ \cos(\omega t)(1 - m_a \sin(\omega t)) - m_a \sin(\omega t) * \cos(\omega t) \} = 0 \quad (3.28)$$

$$\Rightarrow \sin(\omega t) = \frac{1}{2m_a} \quad (3.29)$$

then gives the modulation index for which the ripple is maximum, substituting back in Equation (3.27). The inductance value required to tolerate the ripple is shown in Equation (3.30) :

$$L_i = \frac{V_{Bus}}{4 * F_{sw} * \Delta i_{pp} |_{\max}} \quad (3.30)$$

Capacitor selection:

The output inductor and capacitor form a low pass filter that filters out the switching frequency.

$$F_c = \frac{1}{2\pi\sqrt{LC}} \quad (3.31)$$

$$F_c \leq \frac{F_{sw}}{10} \quad (3.32)$$

$$C = \left(\frac{10}{2\pi F_{sw}} \right)^2 * \frac{1}{L} \quad (3.33)$$

3.9.2 LCL design procedures

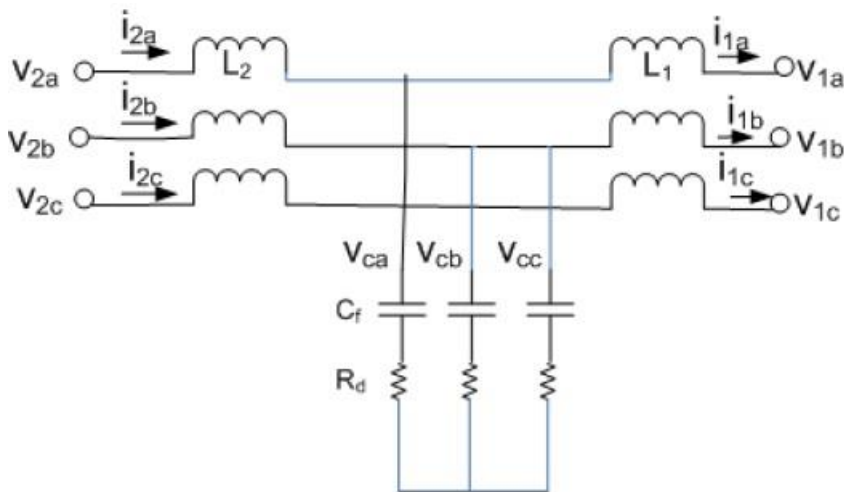


Figure 3.11: LCL Line Filter [23].

The value of LCL filter is chosen as the percentage base value .

Base values:

$$\text{Base Impedance, } Z_b = \frac{Em^2}{p_x} \quad (3.34)$$

$$\text{Base inductance, } L_b = \frac{Z_b}{\omega_n} \quad (3.35)$$

$$\text{Base capacitor, } C_b = \frac{1}{\omega_n * Z_b} \quad (3.36)$$

Where Em is the line voltage, ω_n is the frequency of ac supply, and P_x is the real power consumed by the rectifier.

Converter side inductor L_1 :

Small $L_1 \rightarrow$ High ripple

Large $L_1 \rightarrow$ Low ripple and lower efficiency

$$L_1 = \frac{f_g}{f_{sw}} * \frac{L_b}{THDi} * \sqrt{\frac{\pi^2}{18} \left(\frac{3}{2} - \frac{4\sqrt{3}}{\pi} * ma + \frac{9}{8} * ma^2 \right)} \quad (3.37)$$

Where f_g is grid frequency, f_{sw} is the switching frequency, $THDi$ is Total Harmonic Distortion and ma is modulation index.

Filter capacitor C_F :

The value of the filter capacitor C_F is determined by selecting the reactive power absorbed.

Say X percent of the reactive power (Q) is absorbed at rated values

$$C_F = C_b * X, \quad X \text{ is less than } 5\% \quad (3.38)$$

Grid side inductor L_2 :

$$L_2 = \frac{R_a F_{sw} + 1}{R_a F_{sw} * C_b * \omega_n^2}, \quad R_a F_{sw} = \left| \frac{i_g(s)}{i(s)} \right|_{s=j\omega_s} \quad (3.39)$$

Resonance frequency F_{res} :

$$F_{res} = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 * L_2 * C_F}} \quad (3.40)$$

$$L_T = L_1 + L_2 \leq 0.1L_b$$

Damping Resistor R_d :

The value of damping resistance can be chosen as 25% of capacitor impedance at resonant frequency.

$$R_d = 0.25 * X_c \quad (3.41)$$

4 Implementation of Half bridge converter

The hardware implementation is described in this chapter. All design and implementation are based on the Half Bridge Converter (HBC) for simplicity and cost reduction. The HBC was created such that numerous phases may be joined, enabling the conversion of the HBC from a half bridge to a full bridge or three phases by adding more phases.

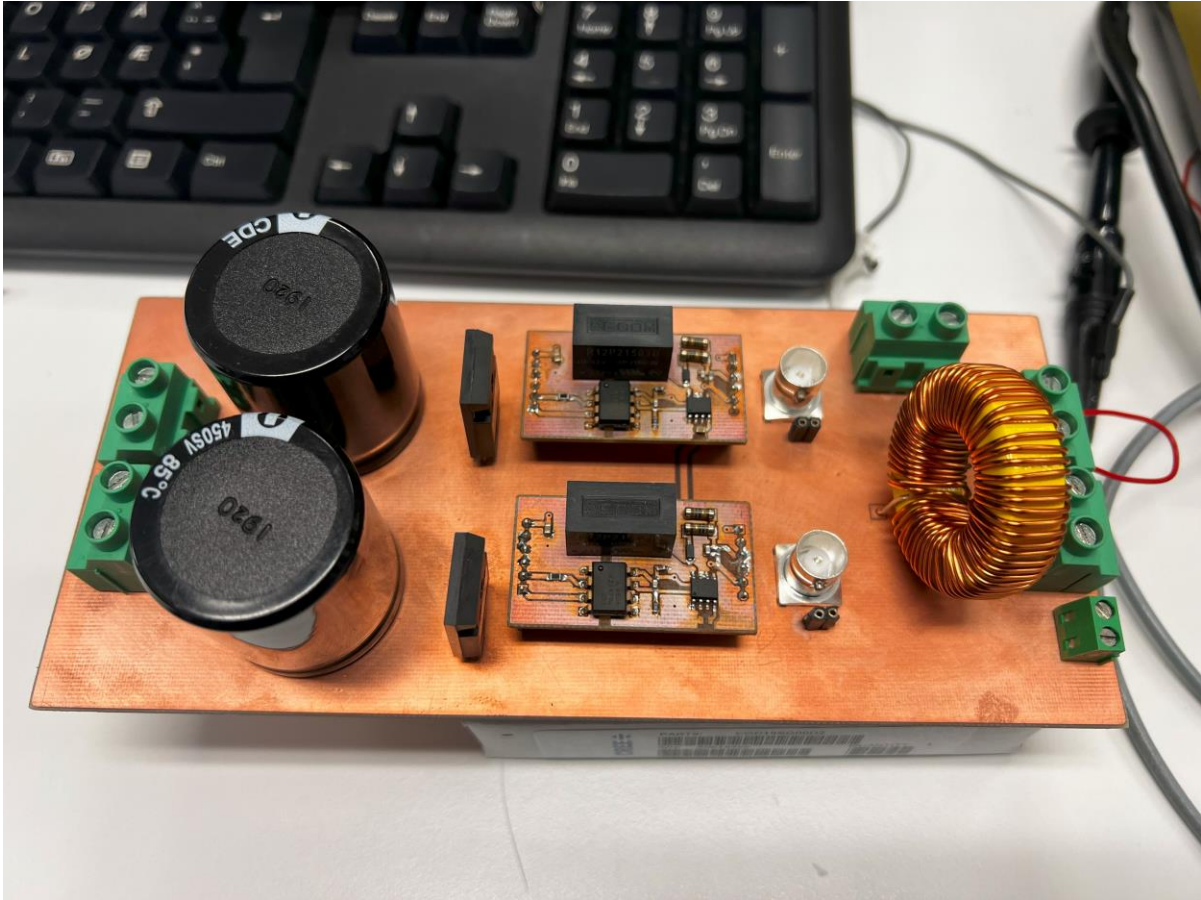


Figure 4.0: Finished design.

As shown in Figure 4.0, the finish design of Half bridge VSC was presented.

4.1 Hardware design

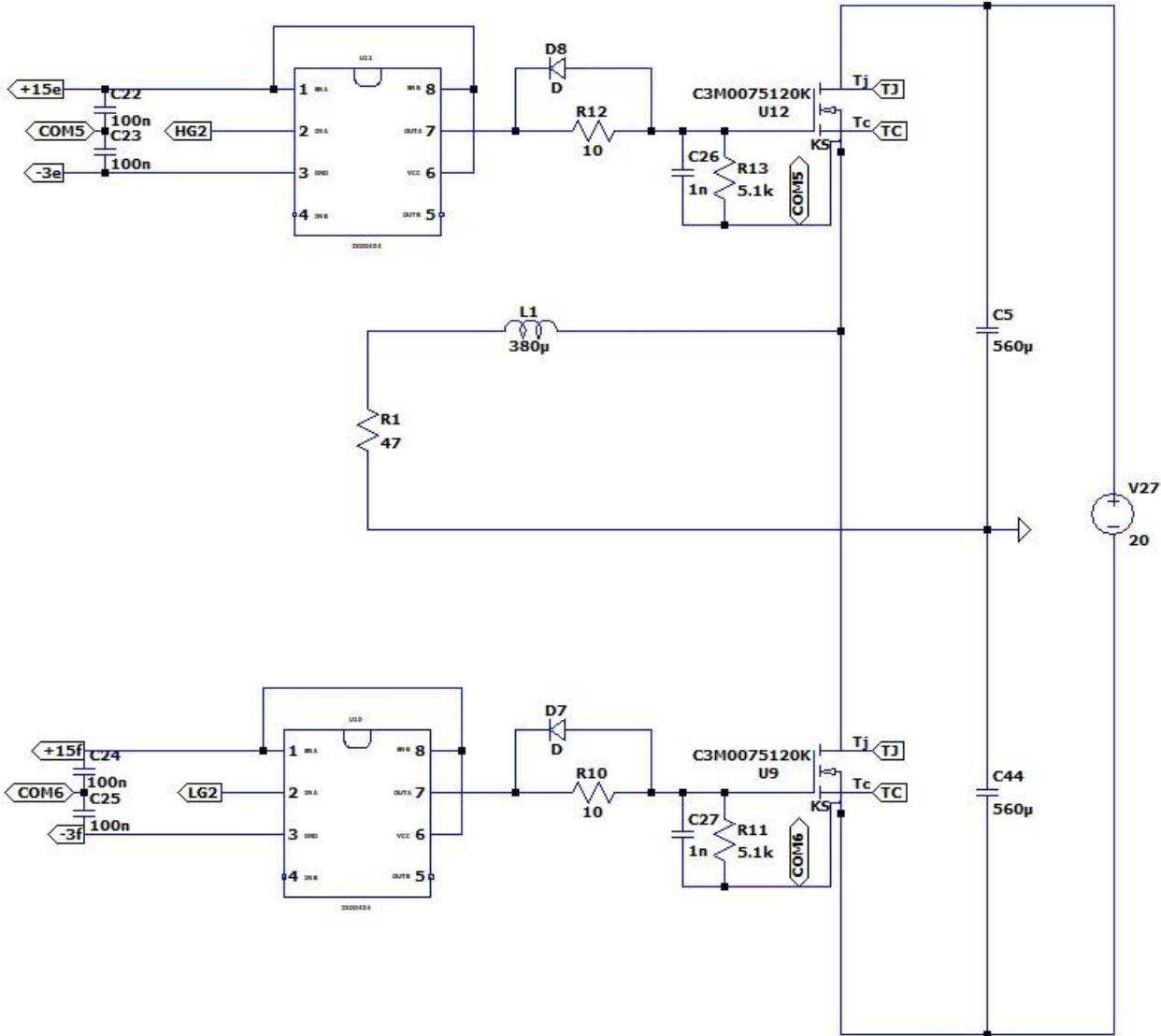


Figure 4.1: Half bridge VSI circuit diagram

In Figure 4.1, an LTspice schematics view of half bridge was presented.

4.2 Components selection

The components for the implementation are based on the design presented in the previous research [3]. The following are the list of components selected for this design.

Table 1: Half bridge converter components.

ITEM	QUANTITY	DESCRIPTION	PART NUMBER	DESIGNATOR
1	2	560 μ F 400 V ,Electrolytic Capacitors	SLPX561M400H7P3	C1
2	4	N-Channel 1000 V 35A (Tc) 113.5W (Tc)	C3M0065100K	Q1,Q2,Q3 and Q4
3	3	Term Blk 2p Side Ent 9.53mm Pcb	1907432	J1,J3 and J14
4	1	Term Blk 2pos Side Entry 5mm Pcb	282836-2	J2
5	6	Conn Bnc Jack Str 50 Ohm Pcb	1-1337445-0	J4,J5,J6,J7,J24 & J25
6	6	Conn Header Vert 2pos 2.54mm	M20-9990246	J8,J9,J24,J27 & J28
7	12	Headers & wire housing 06 Sil Horizontal pin header	M20-9960645	J10-J22

s

ITEM	QUANTITY	DESCRIPTION	PART NUMBER	DESIGNATOR
1	4	4.7 μ f \pm 10% 50V Ceramic Capacitor X5R 0805	GRM21BR61H475KE51L	C1,C2,C5,C7
2	1	Cap Cer 1uf 25v X5r 0603	TMK107BJ105KA-T	C3
3	1	Cap Cer 100pf 50v C0g/Np0 0603	C0603C101J5GACTU	C4
4	1	Cap Cer 1000pf 50v C0g/Np0 0603	GRM1885C1H102JAO1D	C6
5	1	Res 301 Ohm 0.1% 1/8w 0805	ERA6AEB3010V	R1
6	1	Res Smd 20k Ohm 1% 1/10w 0603	RT0603FR E0720KL	R2
7	2	Res Smd 10 Ohm 1% 1w 0207	MMB02070C1009FB200	R3,R5
8	1	Res 5.1k Ohm 1% 1/10w 0603	RC0603FR-075K1L	R4
9	1	Optoiso 3.75kv Open Coll 8dip Gw	HCPL-4506-300E	U1
10	1	Ic Gate Drvr Low-Side 8soic	IXDN609SIATR	U2
11	1	Dc Dc Converter 15v -3v 2w	R12P21503D	U3
12	1	Diode Schottky 40v 1a Sod123	1N5819HW-7-F	D1
13	1	Diode Zener 22v 500mw Sod123	MMSZ22T1G	D2
14	2	Headers & Wire Housing 06 Sil Horizontal Pin Header	M20-9960645	J1,J2

4.3 PCB Design

Proteus software was used in designing the PCB model of the rectifier board and gate driver board according to [3].

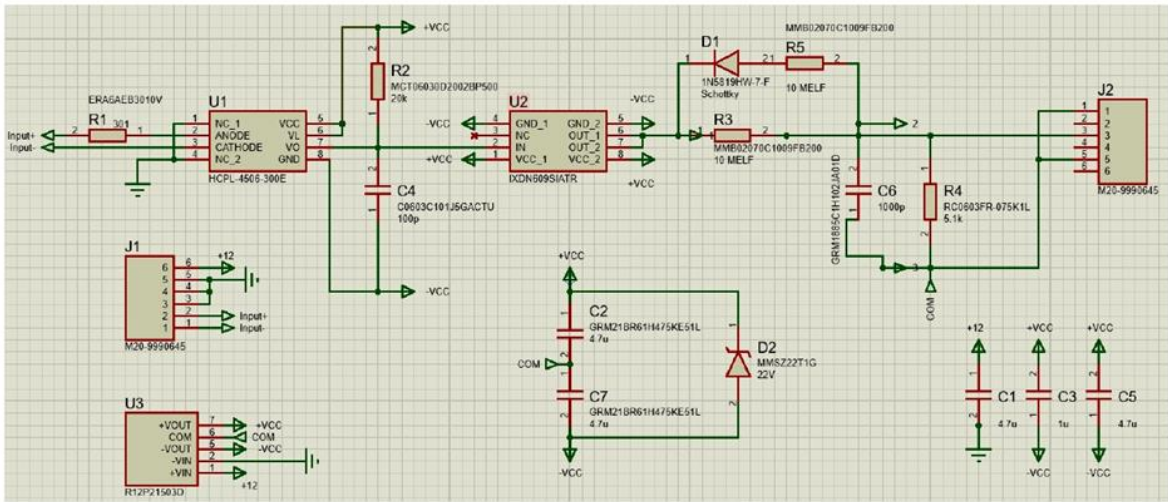


Figure 4.2: Proteus Schematic of gate driver board [3].

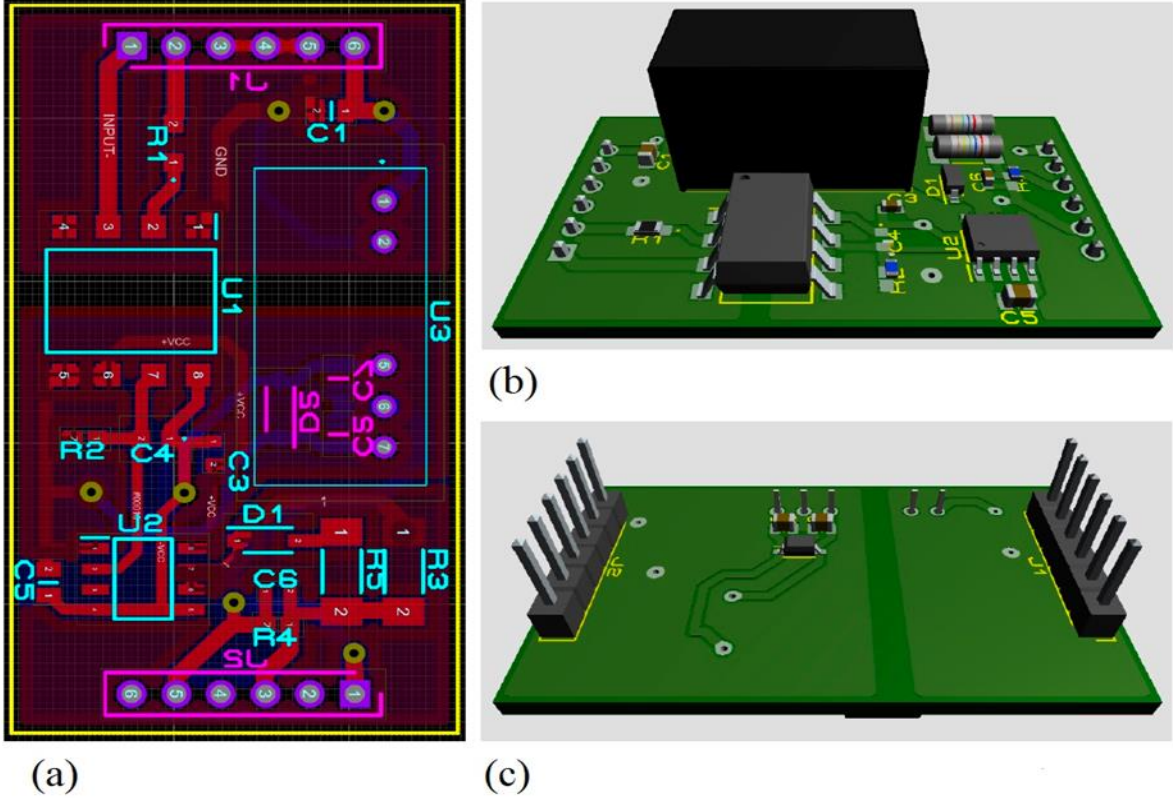


Figure 4.3: (a) PCB board for the gate driver circuit. (b) 3D of the top-view. (c) 3D of the bottom view [3].

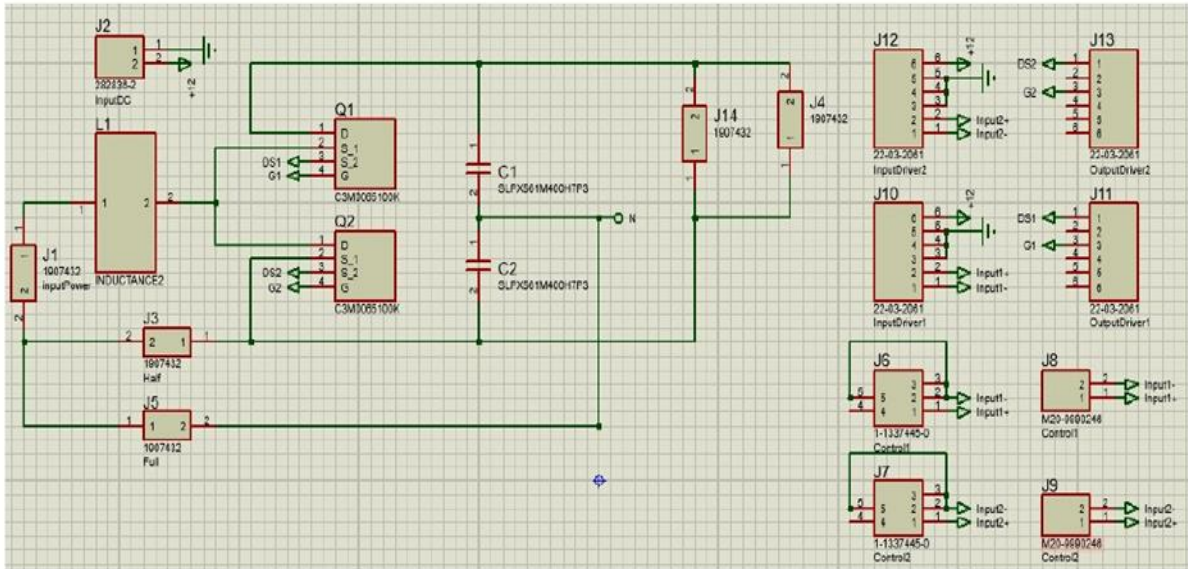


Figure 4.4: Proteus Schematic of inverter board [3].

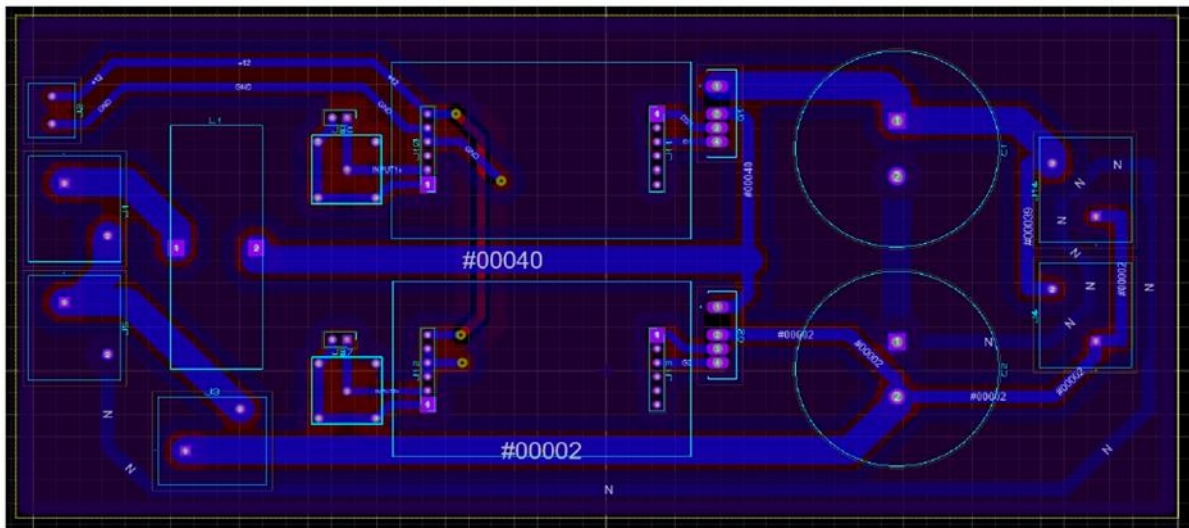
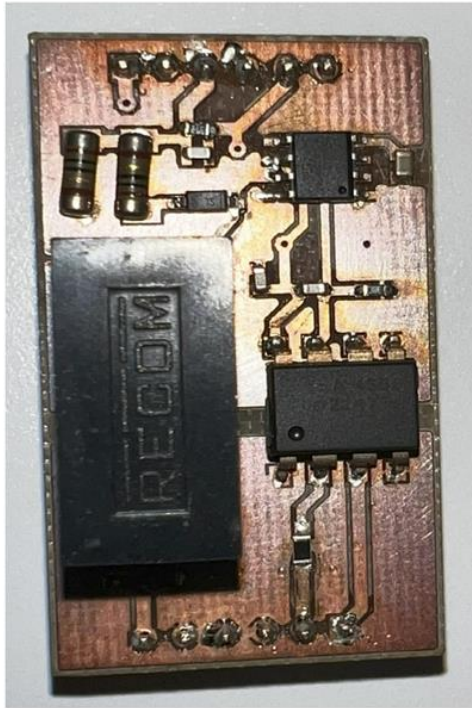


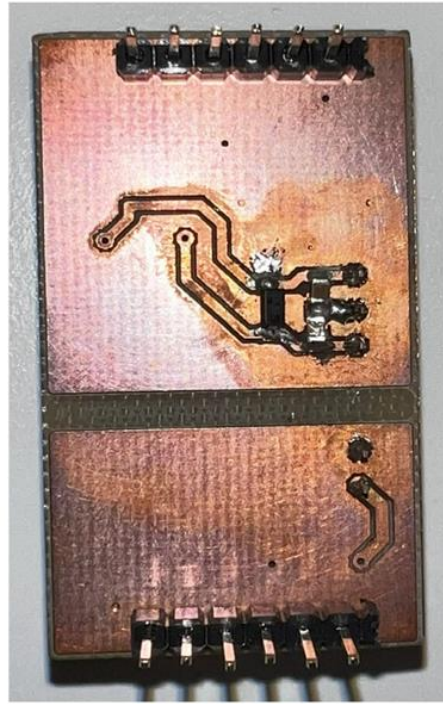
Figure 4.5: Layout of inverter board [3].

4.4 Assembly

The main board of the rectifier is assembled and soldered by hand, while the gate driver was place and soldered using ProtoFlow S and Protoplace S. Therefore, all placing and soldering are based on the design presented in the previous sub chapter.



(a) Top view



(b) Bottom view

Figure 4.6: Gate driver circuit.



Figure 4.7: Half bridge bidirectional DC-AC converter.

5 Experimental verification for Half bridge converter

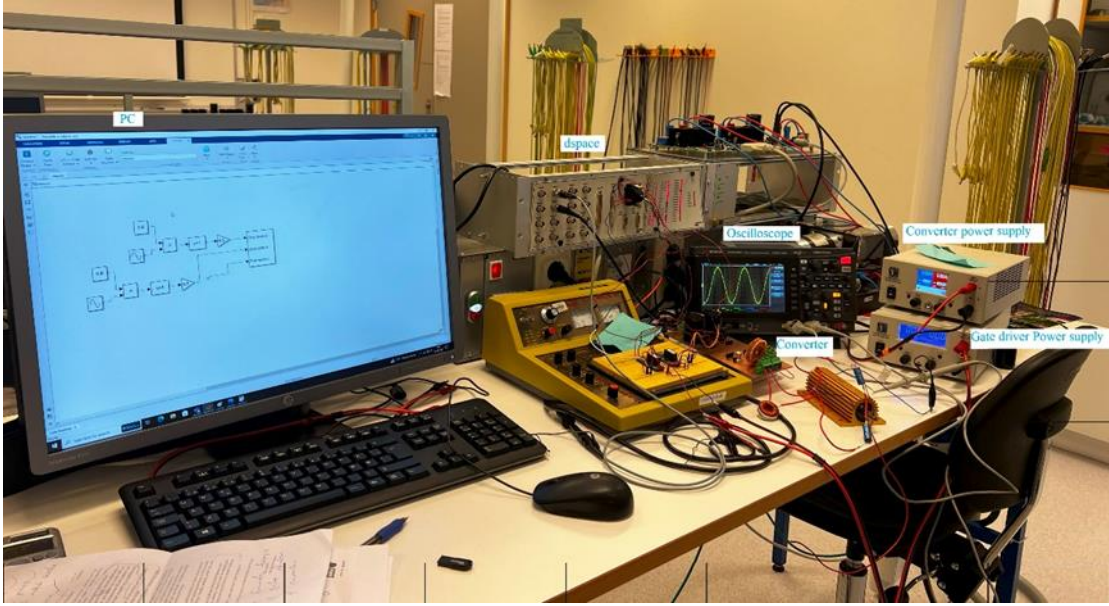


Figure 5.0: Experimental Setup of DC-AC Converter

5.1 Equipment

Table 3: List of equipment's used in the experiment.

S/N	EQUIPMENT	QUANTITY
1	Desktop PC with dSPACE1104	1
2	Oscilloscope	1
3	Power Supply	2
4	Multimeter	1
5	Half bridge bidirectional AC/DC converter	1
6	Gate driver circuit	2

5.2 SPWM Generation

There are several ways of implementing SPWM pulses for HBC, Such as:

- By using DS1104SL_DSP_PWM.
- By using DS1104SL_DSP_PWM3.
- By using Matlab Simulink Blocks.

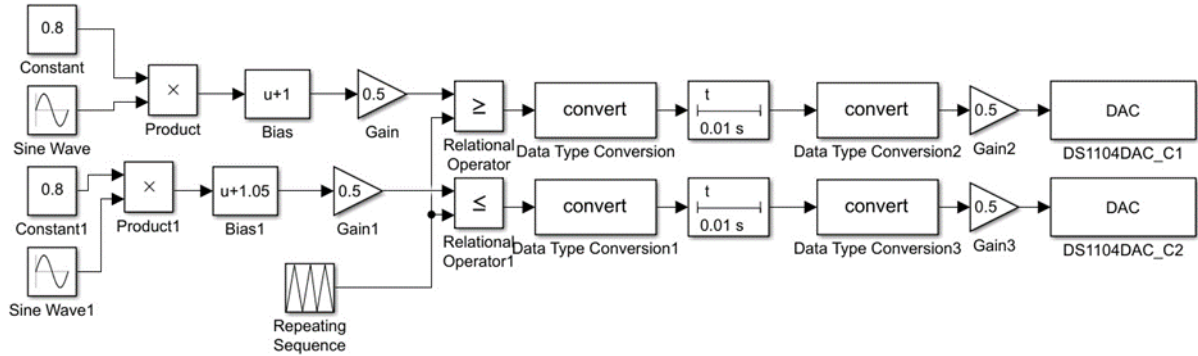


Figure 5.1: SPWM pulses generated by Matlab Simulink Blocks.

Comment: Even though I am able to generate SPWM pulses with deadtime but increasing the frequency above 1kHz generated errors.

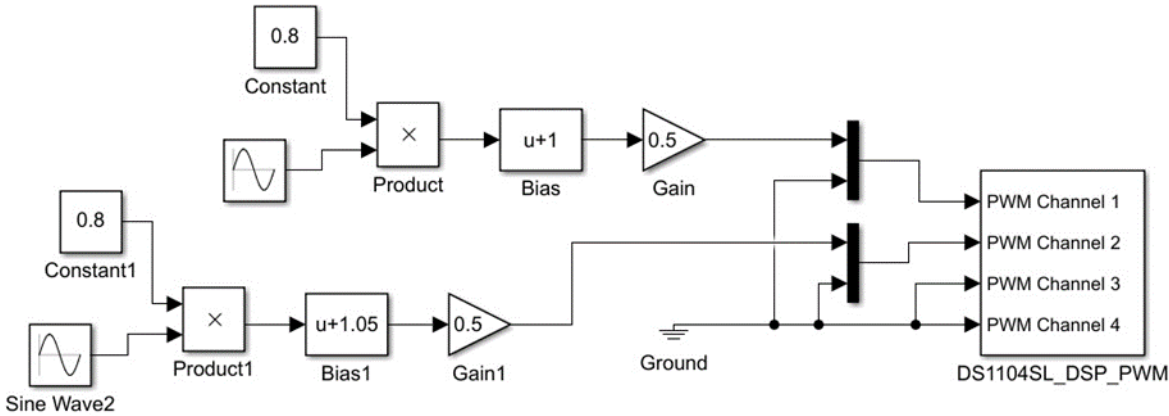


Figure 5.2: SPWM pulses generated using DS1104SL_DSP_PWM.

Comment: The drawback with generating of pulses using this block is difficulty to create deadtime internally. We must attach an external circuit to implement deadtime in our pulses such as TMS320F2812.

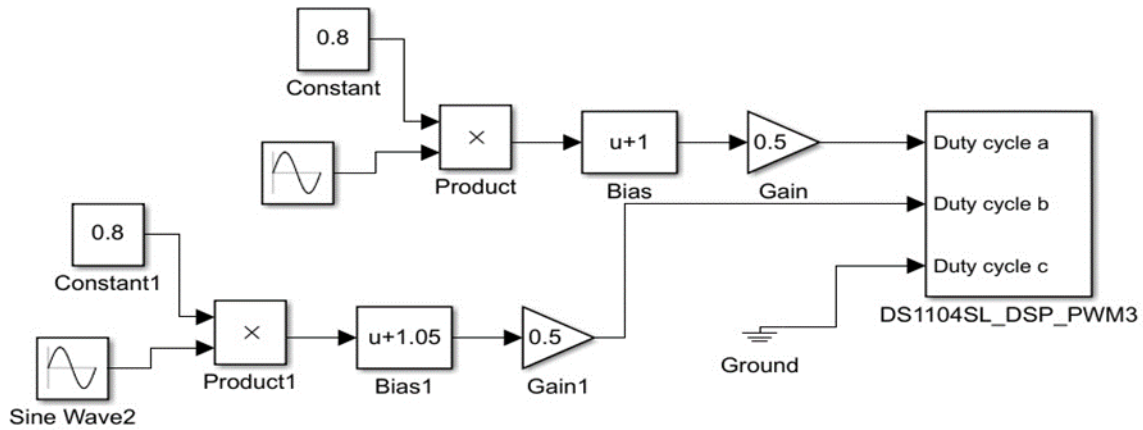


Figure 5.3: SPWM pulses generated using DS1104SL_DSP_PWM3.

Comment: The advantage of this setup is opportunity to increase the frequency above 1kHz and able to implement deadtime. In addition, I am able to invert the SPWM pulses generated.

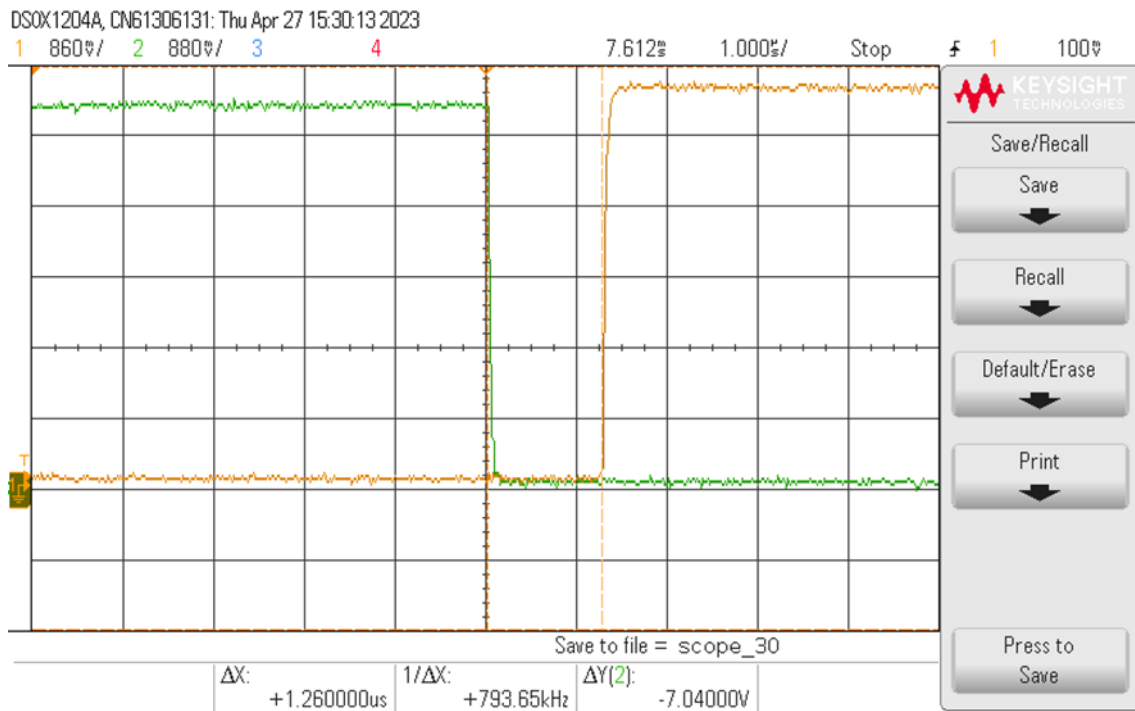


Figure 5.4: Output pulses of the gate driver circuit with deadtime.

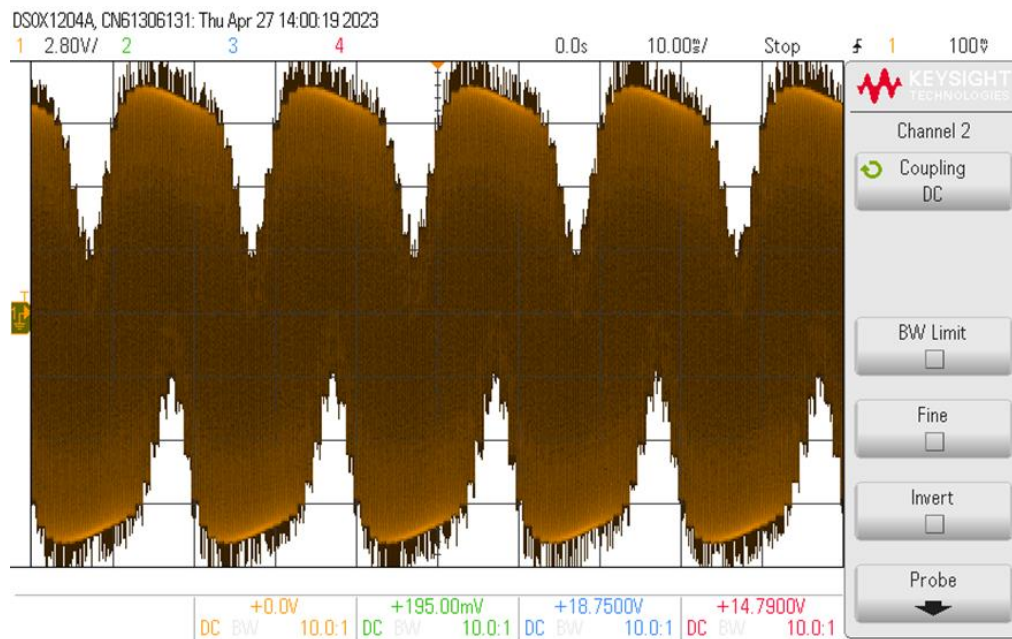


Figure 5.5: Output voltage of the converter.

Comment: The converter was built and test but as shown in figure 5.5 the output contains a lot of ripples , its necessary to develop filter for the converter.

5.3 LC filter design for Half bridge

The procedures for filter design are mentioned in chapter 3.9, the following are the inductor and capacitor values choosing after the design

$$L = 1.46\text{mH}$$

$$C = 50\mu\text{F}$$

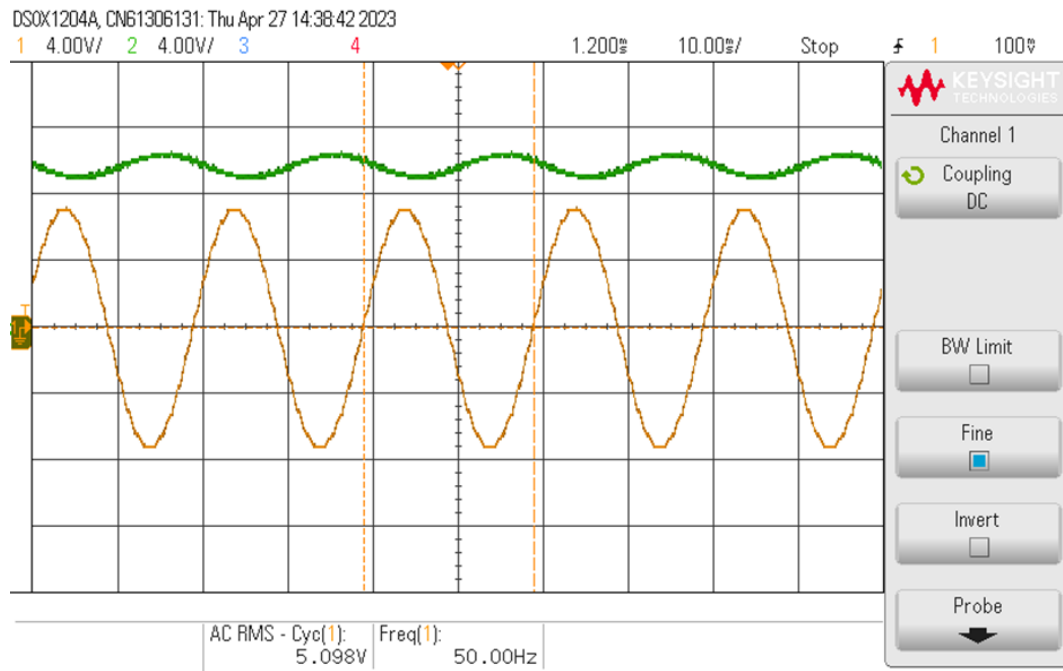


Figure 5.6: Input and Output voltage of the converter after filter design.

6 Hardware design and implementations for 3 phase Voltage source converter

This chapter describes how the creation of an LCL filter enhanced the three-phase converter from earlier research. Additionally, it describes the design process for the PCB.

6.1 Spice simulation for 3 phase voltage source converter

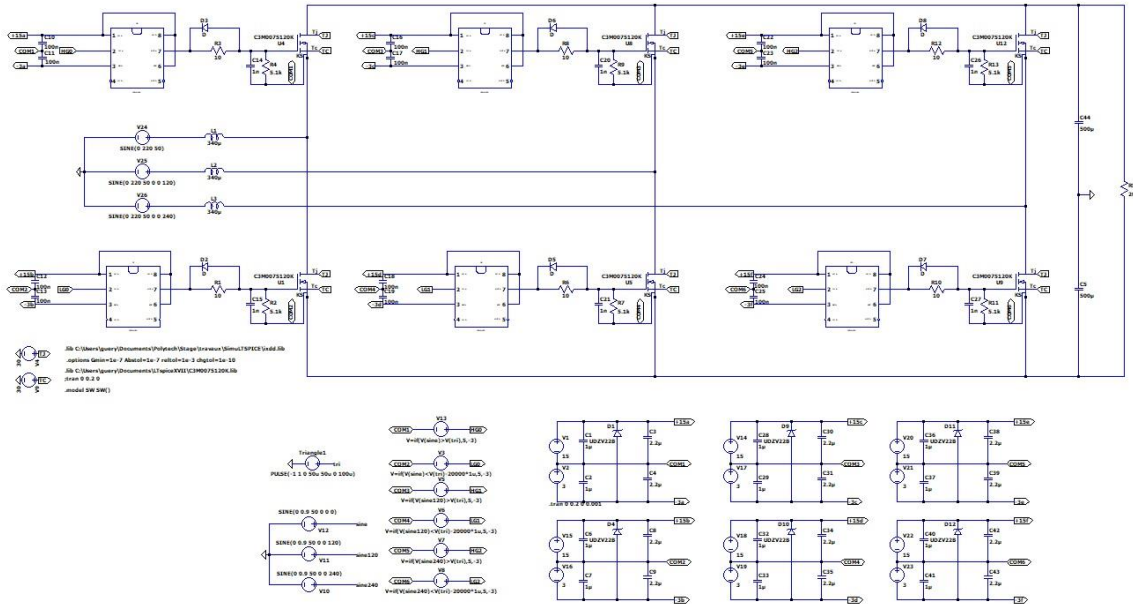


Figure 6.0: Three - phase voltage source converter.

The three-phase converter shown in Figure 5.0 was designed by a former student [1]. as seen in figure 6.1 the input have a lot of harmonic from the AC side which result in instability of the converter.

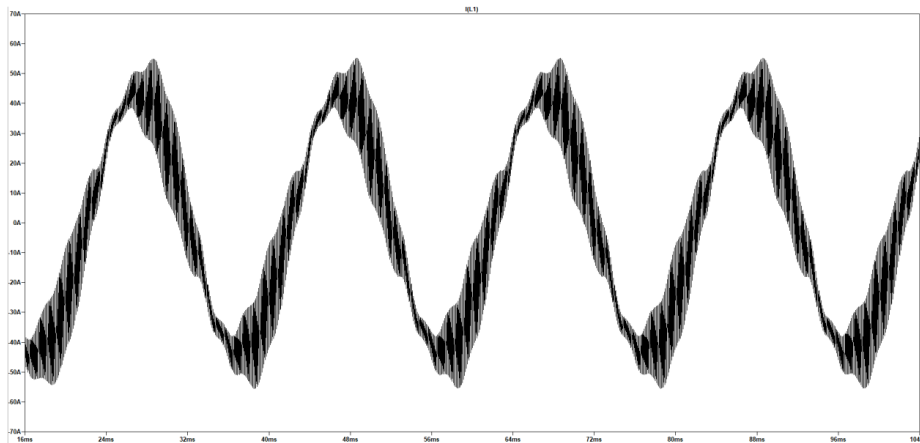


Figure 6.1: Input AC current [3]

6.2 LCL filter design

The filter was create based on the formulation described in chapter 3, the following are the filter values.

$$L_1 = 3.5\text{mH}$$

$$C_F = 4.25\mu\text{F}$$

$$L_2 = 0.55\text{mH}$$

$$R_d = 4.5\text{ohms}$$

After designing the filter, the waveform was improved as shown in the figure below.

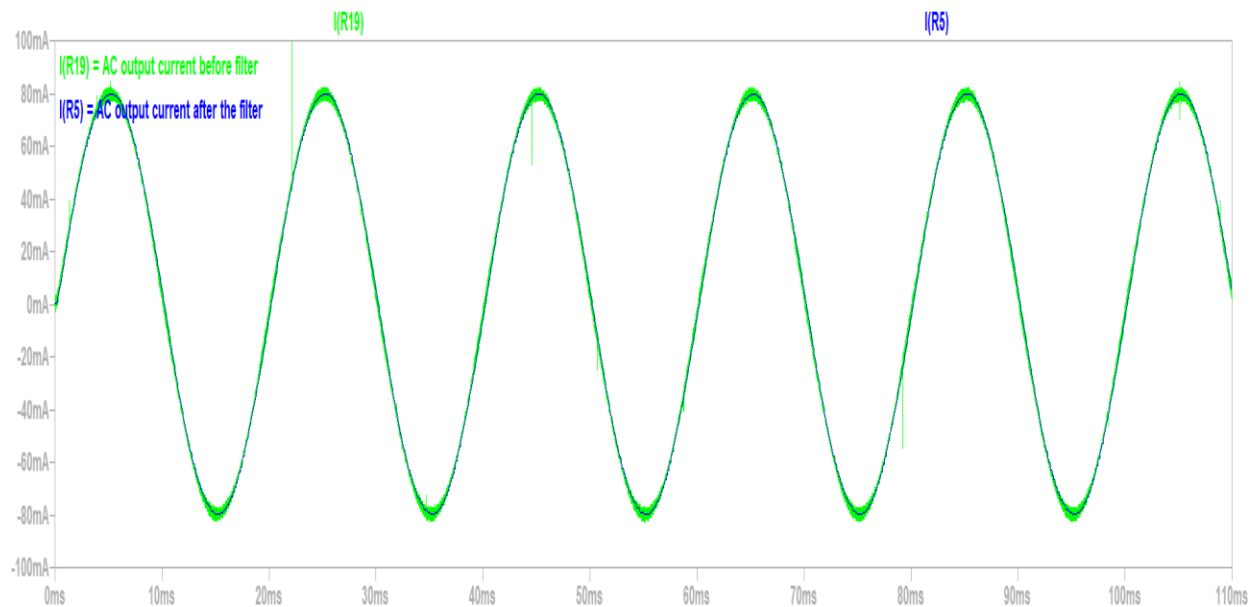


Figure 6.2: improved wave form of input AC current with LCL filter.

As shown in Figure 6.2, the LCL filter was able to filter the output ripples.

6.3 PCB design

Table 4: Three-phase converter components.

ITEM	QUANTITY	DESCRIPTION	PART NUMBER	DESIGNATOR
1	2	560 μ F 400 V ,Electrolytic Capacitors	SLPX561M400H7P3	C1
2	4	Mosfet N-Channel 1000 V 35A (Tc) 113.5W (Tc)	C3M0065100K	Q1,Q2,Q3 and Q4
3	3	Term Blk 2p Side Ent 9.53mm Pcb	1907432	J1,J3 and J14
4	1	Term Blk 2pos Side Entry 5mm Pcb	282836-2	J2
5	6	Conn Bnc Jack Str 50 Ohm Pcb	1-1337445-0	J4,J5,J6,J7,J24 & J25
6	6	Conn Header Vert 2pos 2.54mm	M20-9990246	J8,J9,J24,J27 & J28
7	12	Headers & wire housing 06 Sil Horizontal pin header	M20-9960645	J10-J22

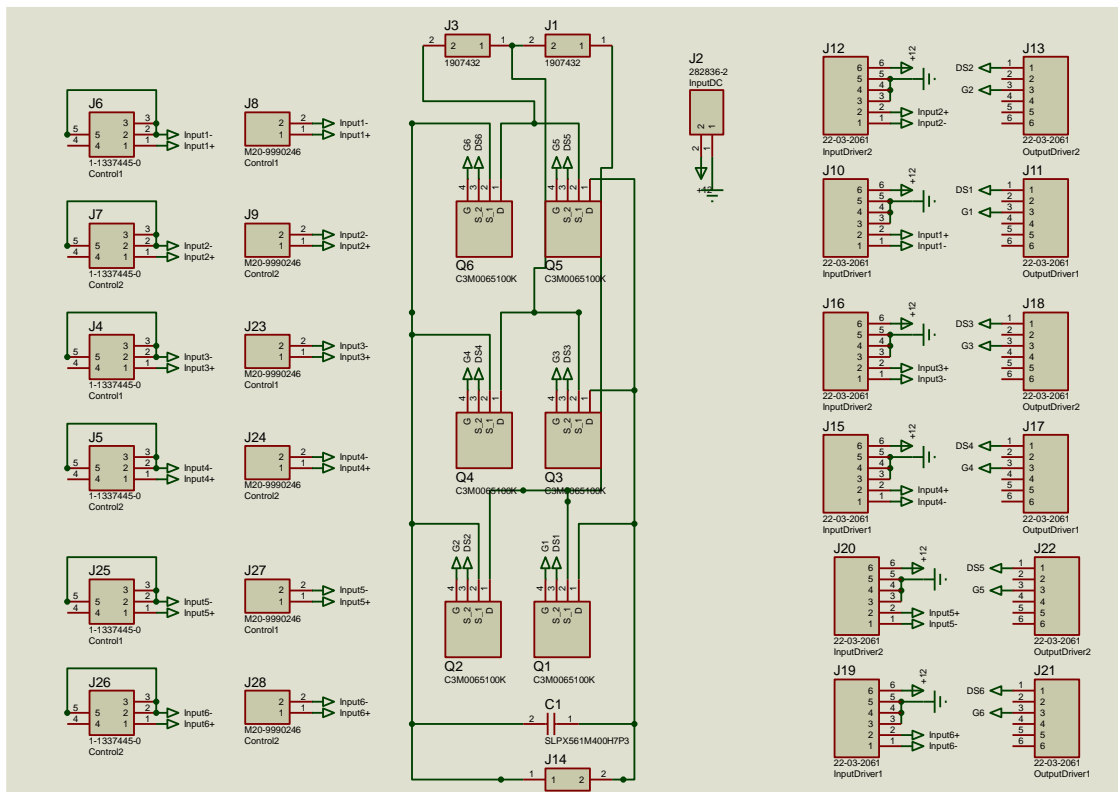


Figure 6.3: Schematic view of three phase voltage source converter

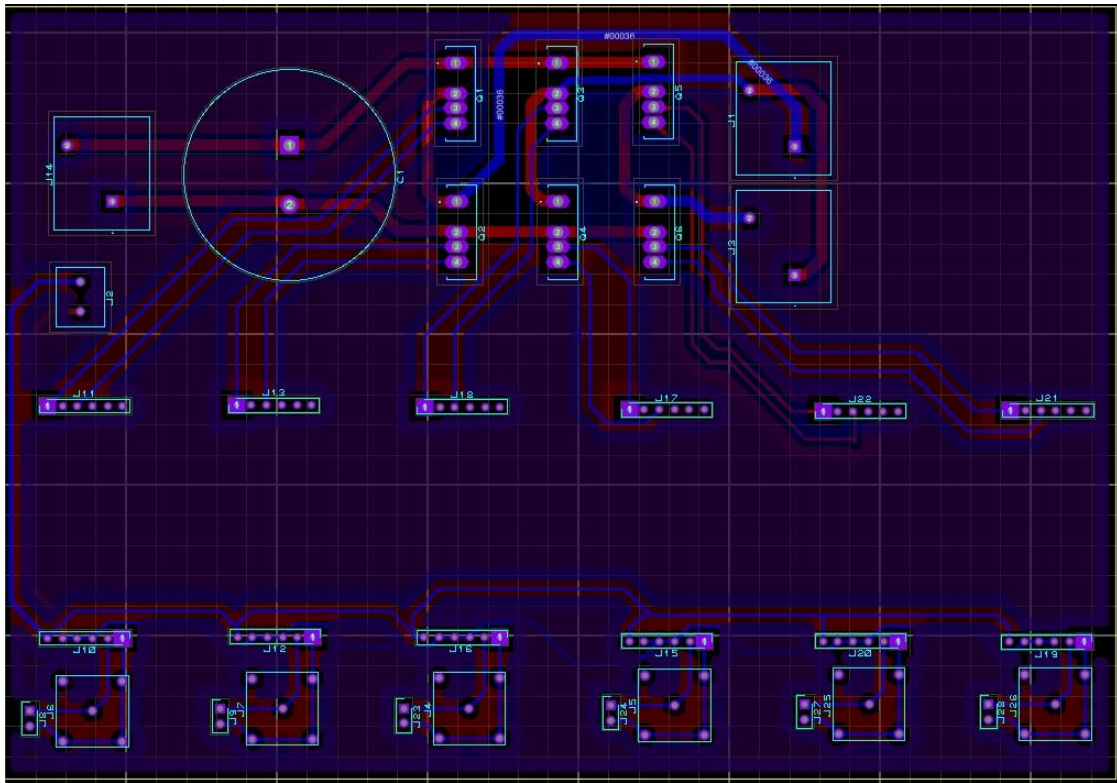
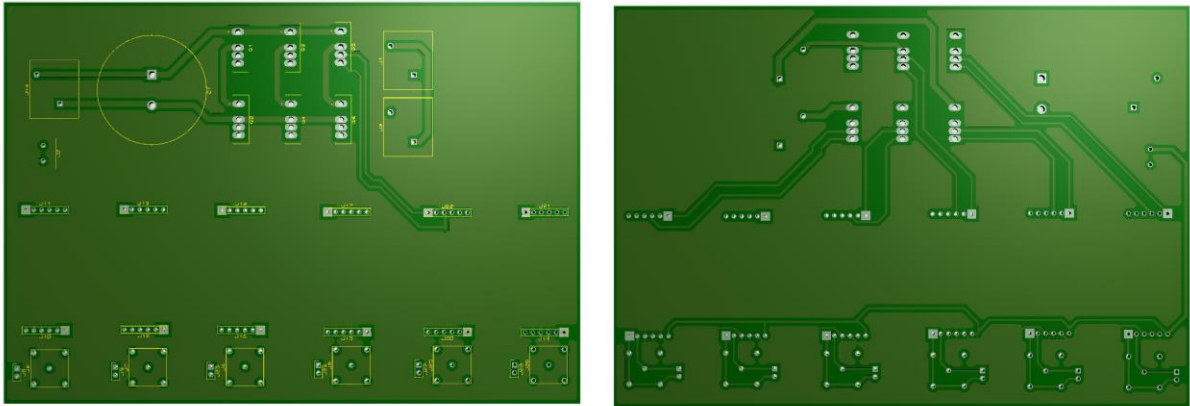


Figure 6.4: PCB design of the three-phase voltage source converter



(a) TOP-VIEW

(b) BOTTOM-VIEW

Figure 6.5: 3D view of the top and bottom view of the PCB

6.4 SPWM generation

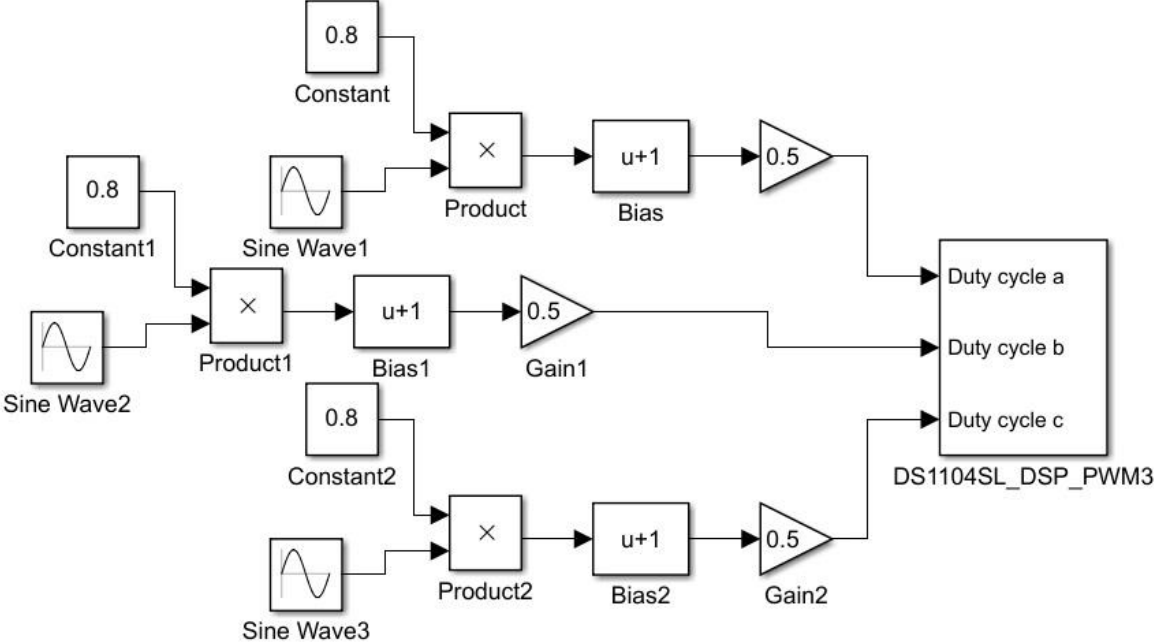


Figure 6.6: Three-phase SPWM generation in dSPACE

7 Analysis on Half bridge converter

7.1 Effect of dead time on the performance of the AC side voltage

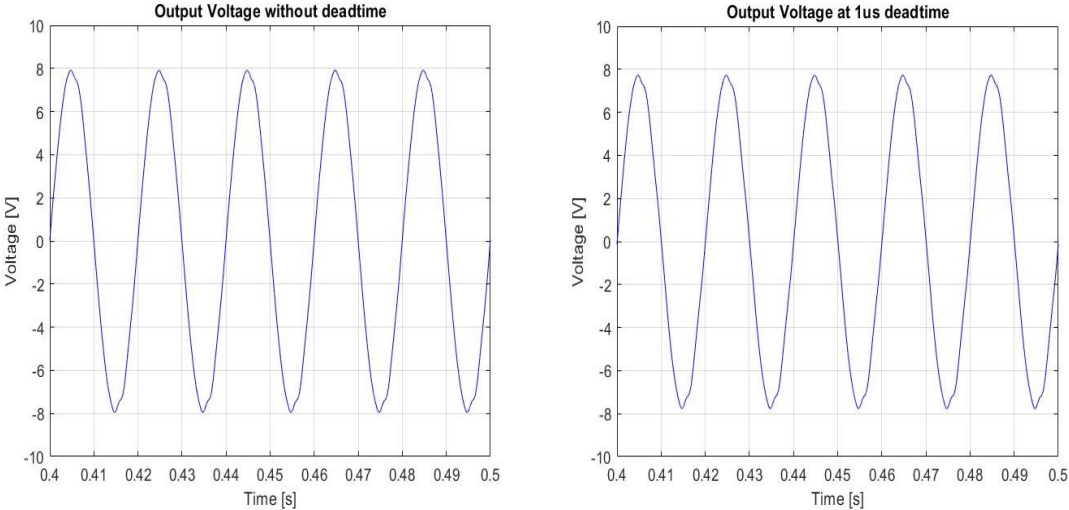


Figure 7.0: (left) Output AC voltage without dead time, (right) Output AC voltage with 1us dead time.

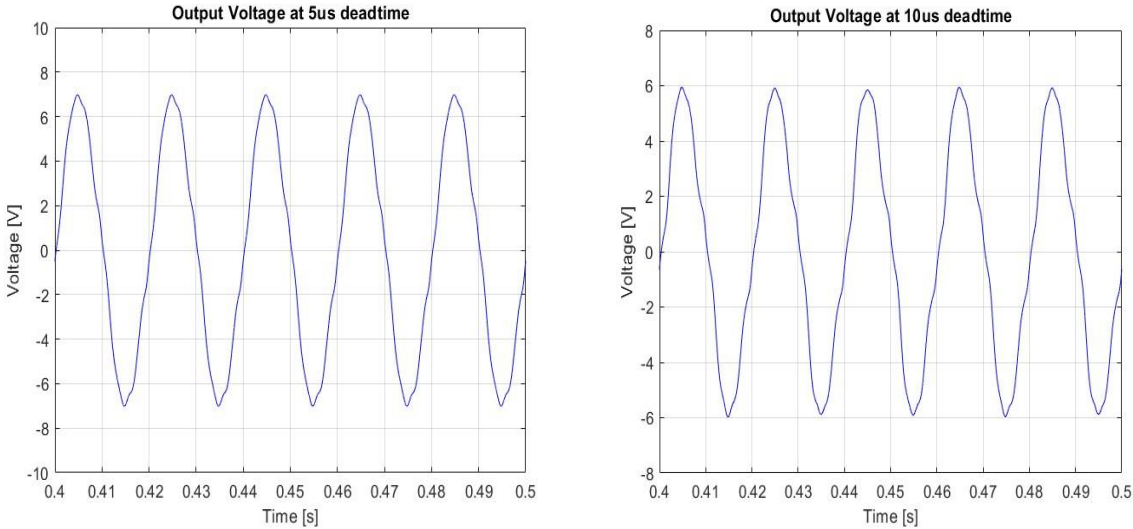


Figure 7.1: (left) Output AC voltage with 5us dead time, (right) Output AC voltage with 10us dead time.

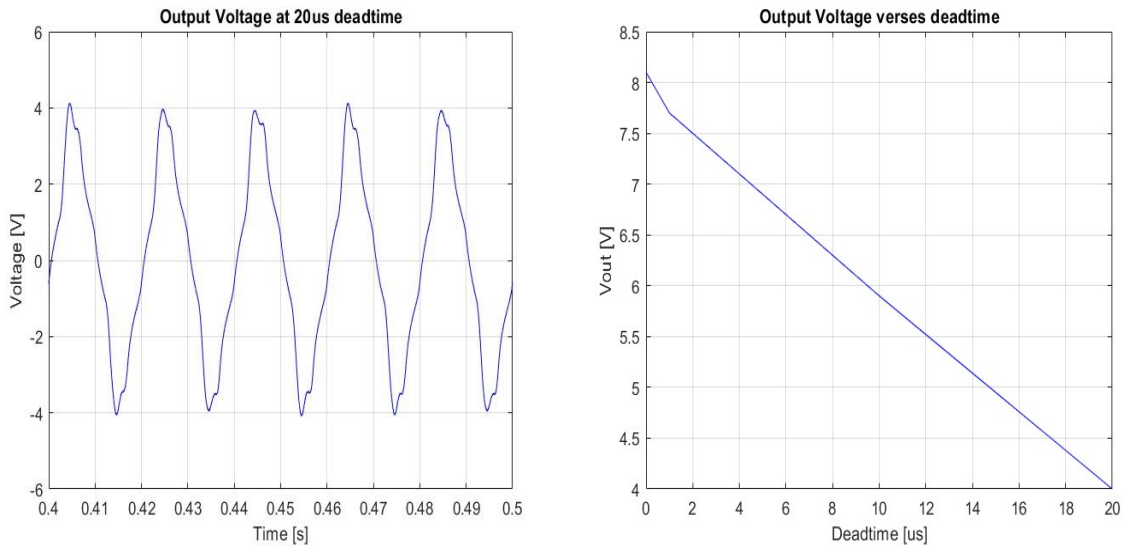


Figure 7.2: Vac at 20us deadtime.

Table 5.0: Shows table of deadtime with AC voltage.

DEADTIME	AC SIDE VOLTAGE
0	8.1
1	7.7
5	6.9
10	5.9
20	4.0

During the dead time, the load will be isolated from the source. But dead time decreases the amplitude of AC voltage, and it deteriorates the shape and quality. If the dead time is increased, it results in a longer period where both switches are off.

In addition, increasing the dead time can also increase the switching losses in the converter,

Overall, increasing the dead time in a voltage source converter should be done carefully, considering the trade-offs between improved switch protection and potential negative effects on the output waveform and efficiency.

7.1.1 Relationship between offset and Deadtime

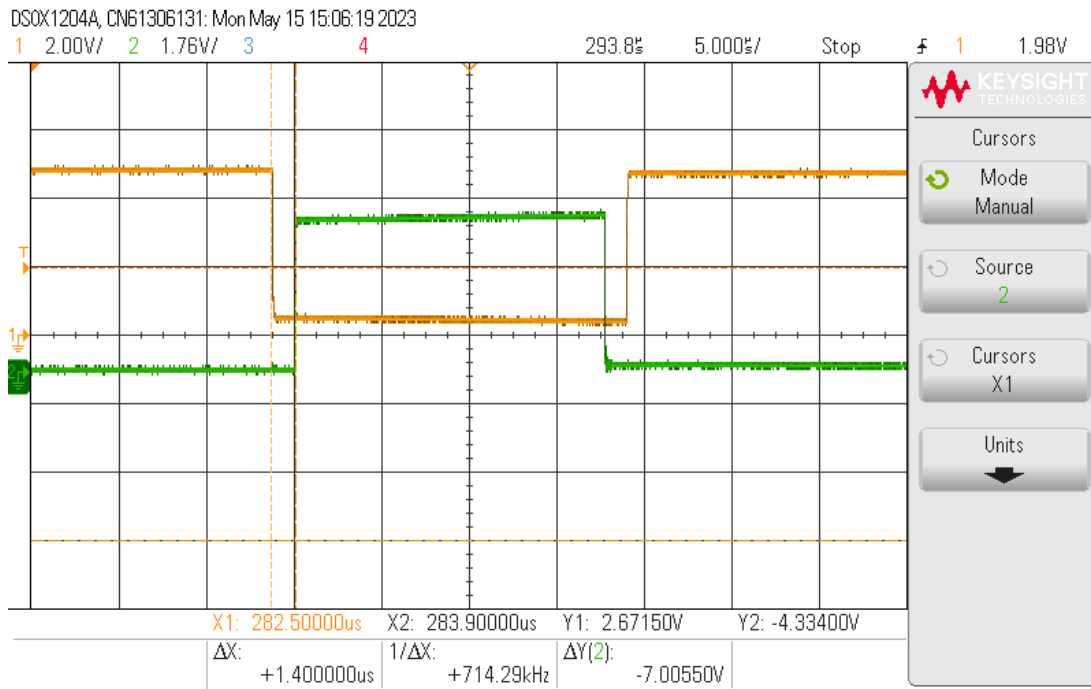
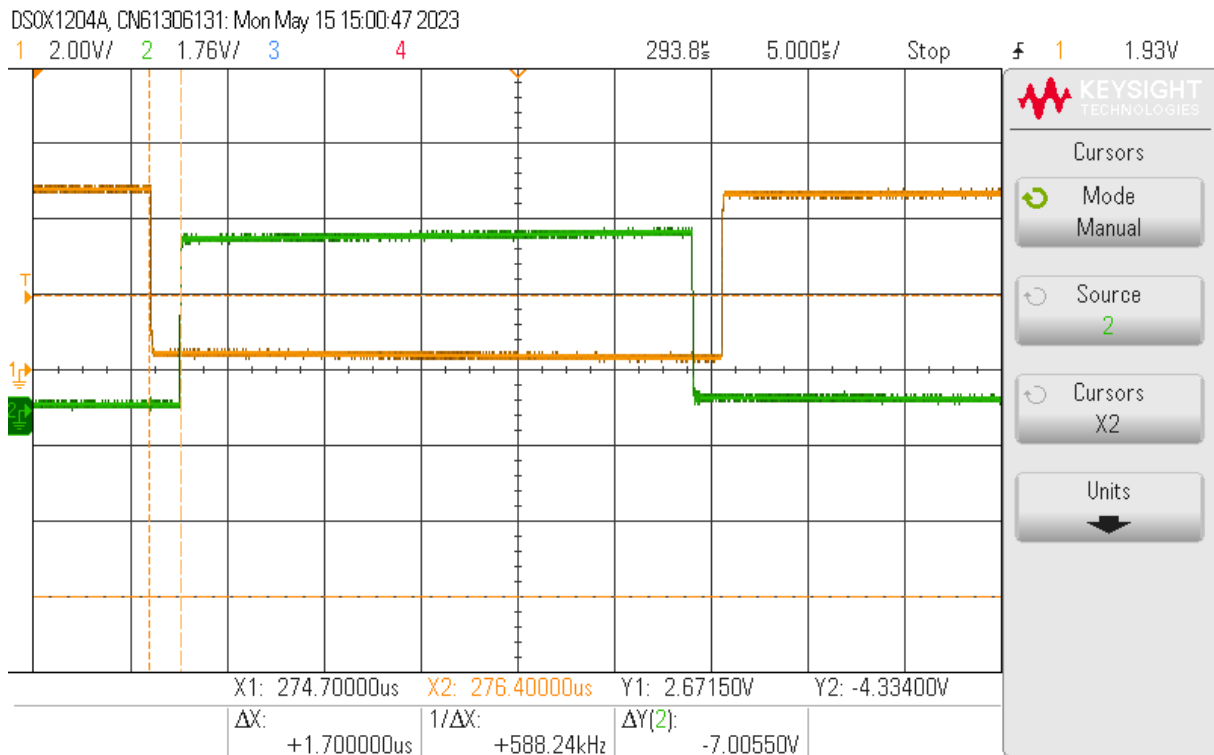


Figure 7.4: 1.4us deadtime at 0.05 offset



7

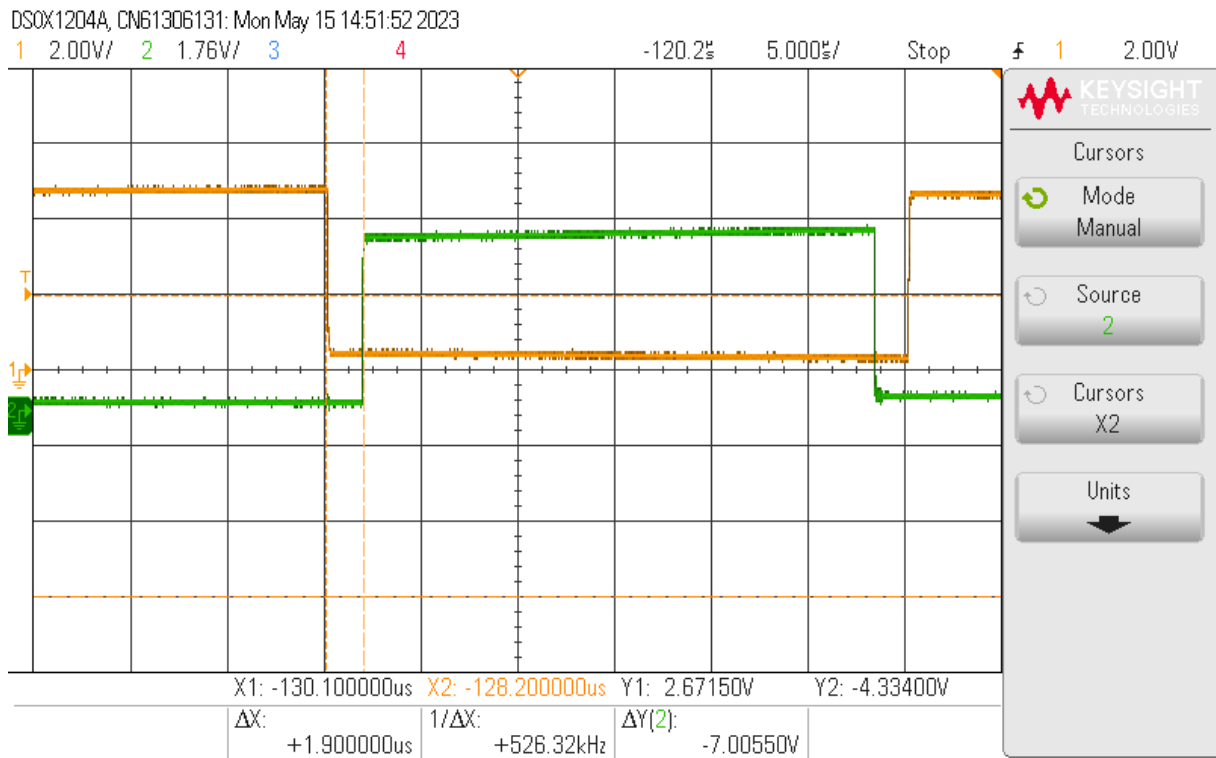


Figure 7.6: 1.9us deadtime at 0.07 offset.

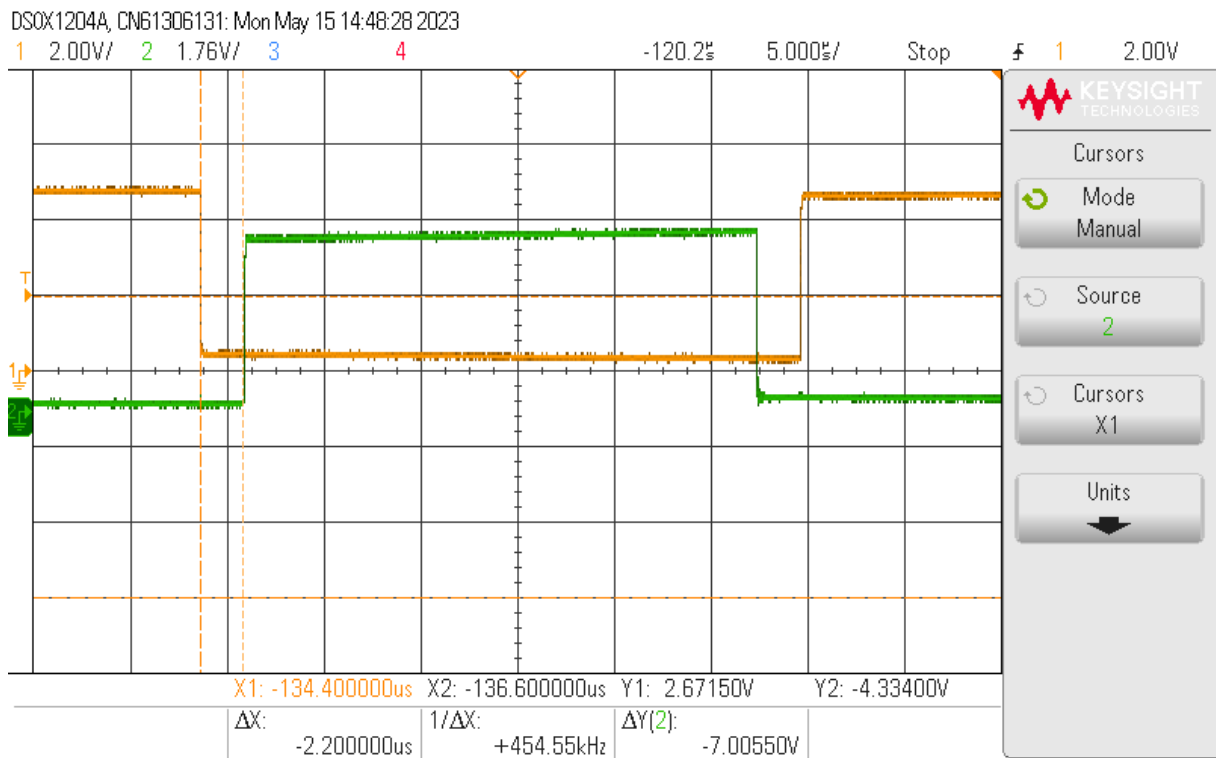


Figure 7.7: 2.2us at 0.09 offset.

Figure (6.6 - 6.9) shows how the deadtime increase with increase in the offset.

7.2 Effect of smaller value of DC link capacitors on the AC side voltage

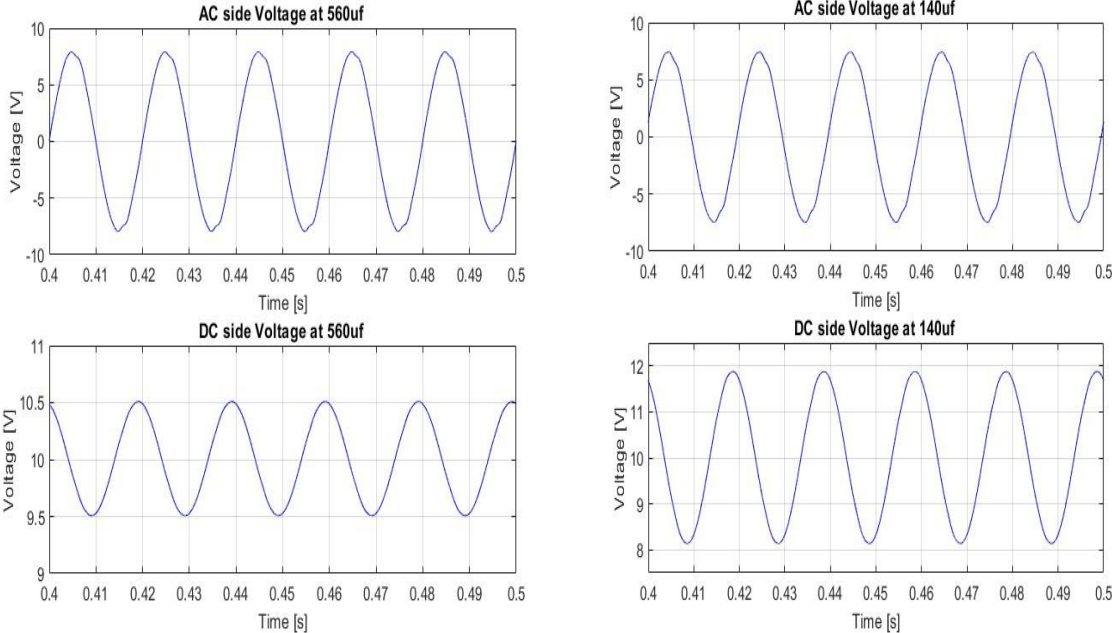


Figure 7.8: AC side and DC voltages at 560uf and 140uf

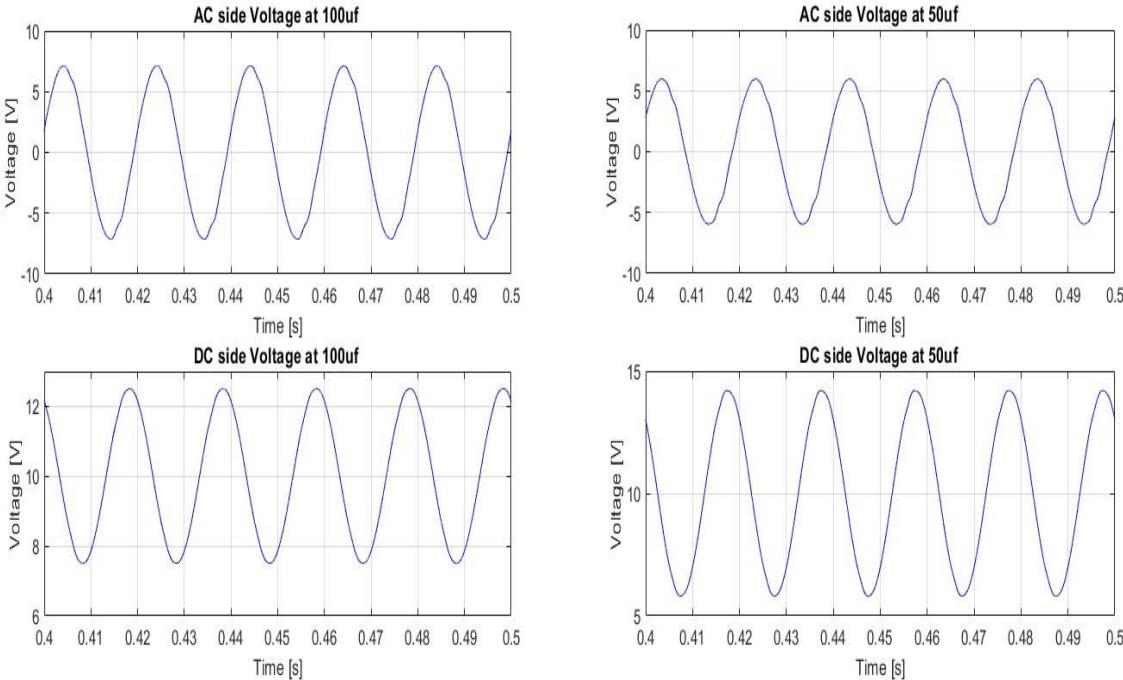


Figure 7.9: AC side and DC voltages at 100uf and 50uf

Lowering the DC link capacitor on a voltage source converter (VSC) can result in a number of different effects, including:

1. **Increased voltage ripple:** The DC link capacitor serves to smooth out the voltage ripples caused by the switching of the VSC. A lower DC link capacitor will result in higher voltage ripple, which can affect the performance of the VSC and the connected system.
2. **Reduced voltage stability:** The DC link capacitor also plays a role in maintaining the stability of the DC voltage supply for the VSC. With a lower DC link capacitor, the voltage stability may decrease, leading to problems such as voltage sag and voltage dip.
3. **Increased stress on switching devices:** Switching devices such as IGBTs or MOSFETs may experience increased stress due to higher voltage ripple and reduced voltage stability.
4. **Reduced power handling capacity:** A lower DC link capacitor may limit the power handling capacity of the VSC, as it may not be able to supply sufficient energy to the load or absorb regenerative energy from the load.

In summary, lowering the DC link capacitor can have several negative effects on the performance, stability, and reliability of the VSC system. It is therefore important to design the DC link capacitor with the appropriate value for the specific application.

8 Conclusions and recommendations for future work

This chapter briefly described conclusion and future work

8.1 Conclusions

During the thesis a comprehensive model for the design and implementation of a separately excited DC machine was introduced. The literature review on the separately excited DC machine, DC-DC converter, and voltage source converter provided a solid foundation for the research. The successful hardware implementation of a half bridge voltage source converter and the design of a three-phase voltage source converter PCB were achieved. The experiments conducted resulted in improved output, and an analysis was conducted on the half bridge voltage source converter. Overall, this research has contributed to the understanding of the associated converters.

8.2 Recommendations for future work

In this project half bridge converter was implemented and analysis, the next stage was to implement three-phase voltage source converter.

During the analysis, the deadtime effect of deadtime on the performance of the output was investigated, so it's necessary to develop a deadtime compensation in order to overcome the effect of dead time.

Lastly, DC-DC converter can be implemented, tested and analysis could be carry out in other to get the whole model running.

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Annex 1 MOSFET DATA SHEET



C3M0075120K

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

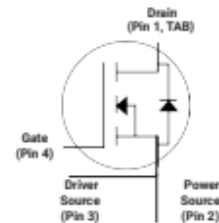
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

V_{DS}	1200 V
$I_D @ 25^\circ\text{C}$	30 A
$R_{DS(on)}$	75 m Ω

Package



Part Number	Package	Marking
C3M0075120K	TO 247-4	C3M0075120K

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC ($f > 1\text{ Hz}$)	Note: 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note: 2
I_D	Continuous Drain Current	30	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 19
		19.7		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}$	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_p limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	113.6	W	$T_c = 25^\circ\text{C}, T_j = 150^\circ\text{C}$	Fig. 20
T_j, T_{stg}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$		
T_L	Solder Temperature	260	$^\circ\text{C}$	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode $V_{GSmax} = -4\text{V}/+19\text{V}$
 Note (2): MOSFET can also safely operate at $0/+15\text{ V}$

