Digital Controller Design and Implementation for AC and DC Side of 3ph qZSI

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***Abstract*—This paper presents the multi-loop digital controller design of a quasi-z-source inverter (qZSI). The qZSI is a single-stage power converter and can operate in buck and boost modes. The qZSI is an economical solution for distributed generation and eliminates the need for two-stage power conversion. This paper proposes a detailed step-wise digital controller design using a multi-loop control method. The controllers of the AC and DC sides are designed separately. A proportional controller is used for the inner current control loop on both the AC and DC sides. In contrast, for outer voltage loop control, the proportional and resonant (PR) controller is used on the AC side, and the proportional and integral (PI) is used on the DC side. In designing the digital controllers, the effect of the sensor gain and low pass filter (LPF) in the feedback path is also considered. Furthermore, to mimic the behavior of the synchronous generator, the droop control is used to generate the reference voltage for the AC side of the controller. The time domain simulations are carried out to verify the designed controllers. Experimental results are also presented for the validation of the proposed controllers.**

***Index Terms*—Digital controller design, droop control, proportional-integral controller, proportional-resonant controller, quasi-z-source inverter.**

I. Introduction

In recent years, there has been a significant increase in research on distributed generation and microgrids, driven by the growing adoption of renewable energy sources (RES) such as solar and wind power. To extract the electrical power from RES in standard form, i.e., fixed voltage and frequency, power conditioning is performed using a voltage source inverter (VSI) or current source inverter (CSI). Further, the inverter studies can be classified into two domains i.e., hardware design and control design. From a hardware design point of view, conventionally, two-stage topology is used to extract the power from variable low DC voltage RES, as variable DC voltage is unsuitable for directly generating a fixed AC output. In this topology, the variable DC voltage is first converted into a fixed high DC voltage using a DC-DC converter. Then, a VSI is employed to convert the fixed high DC voltage into the desired AC output. In some cases, an isolated three-phase transformer is connected to the inverter output to provide galvanic isolation and step up the AC voltage if needed [1], [2].

The two-stage topology is not cost-effective as reported in [2]. The alternate solution of two-stage topology is proposed in [3] as a z-source inverter (ZSI). The ZSI is also known as a single-stage buck-boost inverter [3]. The ZSI utilizes zero vector time intervals to boost the DC-link voltage by shoot-through. Zero vector time interval is defined when all upper or lower switches of the three-phase bridge are turned on. The shoot-through phenomenon occurs when the upper and lower switches of a single leg or all three legs of the three-phase bridge in the ZSI are turned on simultaneously.

The ZSI, despite its advantages, suffers from a drawback of non-continuous input current [4]. This limitation requires the use of capacitors with high capacitance ratings. In contrast, the quasi-Z-source inverter (qZSI) overcomes this issue by enabling continuous input current from a DC energy source. This characteristic allows for utilizing smaller capacitors in the input impedance network, reducing manufacturing costs while ensuring the desired functionality is maintained [4], [5].

From a control point of view VSI and CSI are mainly classified as current control and voltage control inverters. The inverters are also named as voltage-controlled voltage-source inverter (VCVSI), current-controlled voltage-source inverter (CCVSI), voltage-controlled current-source inverter (VCCSI), and current-controlled current-source inverter (CCCSI) [6]–[8]. The closed-loop control of the qZSI is an active area of research. The qZSI has two sides, AC and DC.

On the DC side of qZSI, an indirect control method regulates the DC-link voltage [9]. This is necessary due to the pulsating nature of the DC-link voltage caused by shoot-through intervals. The capacitor voltage in the impedance network is controlled using a proportional and integral (PI) controller in the indirect control method. In [10], the reference for the capacitor voltage is generated by taking the average of the input voltage and the desired DC-link voltage. However, the inductor current in the impedance network is not actively controlled in the previous studies [9]–[12], which may lead to inductor saturation and potential damage.

On the AC side of qZSI, control is performed either using a multi-loop or single-loop control methodology. In multi-loop control, a proportional (P) controller is used as the inner current controller, and a PI or proportional-resonant (PR) controller is employed as the outer voltage loop controller [9], [11]. The advantage of using a PR controller is that it achieves zero steady-state error without requiring computationally intensive reference frame transformations [12]. In single-loop control, PR [13], model predictive control (MPC) [14] and model predictive control using joint voltage vector (MPCVV) [15] are incorporated. However, previous studies [9]–[15] neglected the effects of sensor gain and low-pass filters (LPFs) used in the feedback path, which can cause stability issues in the system.

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Moreover, the digital control design for the qZSI has not been extensively explored. To implement the control algorithm in a digital signal processor (DSP), digital controllers are required. Additionally, the conventional methods for shoot-through pulse generation involve the use of "OR" gate ICs to combine the AC and DC controller outputs or fully software-based solutions [9], [14].

In this paper, modeling of AC and DC sides are done separately to design the controller for each side. On the DC side, the inner current control loop employs a proportional controller, while the capacitor voltage control loop is designed using a PI controller. The AC side controller is designed in a stationary reference frame, with a proportional controller in the inner current control loop and a proportional-resonant (PR) controller in the outer AC voltage control loop. The feedback signals in the control loops include the sensor gain and low-pass filter (LPF) which effects the system stability. These stability issues are considered in designing the controllers. This paper also introduces a two-timer method to reduce the computation and complexity in the pulse generation form controller. Furthermore, droop control is incorporated to emulate the behavior of a synchronous generator, which determines the reference for the AC-side voltage control loop. Finally, the designed digital controller is verified through time domain simulations and experimental results. The main contributions of this paper are summarized as follows:

- Multi-loop indirect control on DC side.
- While designing the AC and DC side digital control, sensor gain and LPF are considered in the feedback path.
- Discretization of the AC and DC side for designing the discrete controllers.
- DSP control implementation algorithm for the multi-loop control with shoot-through capability using two timers.

The remainder paper is divided into five sections. Section II presents the small signal modeling of qZSI. Section III describes the step-wise procedure to design the digital control of qZSI. Section IV deals with the controller implementation in a digital signal processor (DSP). Section V shows the time domain simulation and the experimental results. Section VI concludes the paper.

II. Small Signal Modeling of qZSI

Fig. 1 shows the three-phase voltage-controlled voltage-source qZSI. The small signal modeling of the AC and DC sides is done separately to have different controllers on each side. The DC side controller response is slower than the AC side controller [9], [16]. The AC and DC controller response speed difference decouples both side dynamics. The modeling of the AC and DC side helps in designing the controllers. In the following sub-section, the AC and DC side modeling is explained.

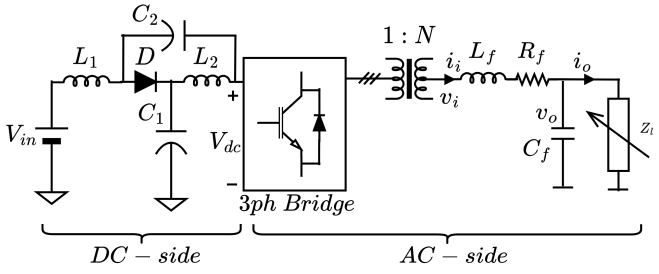

Fig. 1. Basic three-phase voltage-controlled voltage source qZSI.

A. AC Side Modeling

The modeling of AC side qZSI is similar to the well-developed literature for the three-phase inverter. The modeling is performed in stationary $\alpha\beta$ reference frame at the secondary side of the transformer. The advantage of modeling in stationary $\alpha\beta$ reference frame is the non-existence of any coupled terms as in the synchronous dq reference frame case. The AC side dynamic equations (1) and (2) for the three-phase system in $\alpha\beta$ reference frame are derived by applying Kirchhoff's voltage law (KVL), and Kirchhoff's current law (KCL) for each "x" $(x = \alpha, \beta)$ [1].

$$L_f \frac{\partial i_{ix}}{\partial t} + R_f i_{ix} = v_{ix} - v_{ox} \tag{1}$$

$$C_f \frac{\partial v_{ox}}{\partial t} = i_{ix} - i_{ox} \tag{2}$$

where L_f, R_f, and C_f are filter inductance (equivalent transformer leakage inductance), filter resistance (equivalent transformer resistance), and filter capacitance, respectively. i_{ix}, v_{ix}, v_{ox}, and i_{ox} are inverter current, inverter pole voltage, capacitor voltage, and load current, respectively. Further, the inverter voltage and modulation index required to get the desired output AC voltage are related as (3).

$$v_{ix} = \frac{V_{dc}}{2} \cdot N \cdot m_x \tag{3}$$

where V_{dc}, N, and m_x are DC bus voltage, transformer turns ratio, and modulation index, respectively. The AC side model in continuous domain shown in Fig. 2 is developed by applying Laplace transform on (1) and (2) and combining with (3). From Fig. 2, the filter inductor current and output capacitor voltage transfer functions are derived using Mason's rule.

$$G_{ix}^{ac}(s) = \left.\frac{i_{ix}}{m_x}\right|_{i_{ox}=0} = \frac{V_{dc}}{2} \cdot N \cdot \frac{C_f s}{L_f C_f s^2 + R_f C_f s + 1} \tag{4}$$

$$G_{cx}^{ac}(s) = \left.\frac{v_{ox}}{i_{ix}}\right|_{i_{ox}=0} = \frac{1}{C_f s} \tag{5}$$

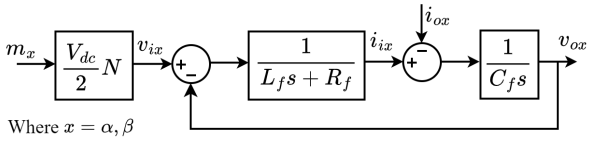

Fig. 2. AC side model block diagram of qZSI in $\alpha\beta$ reference frame.

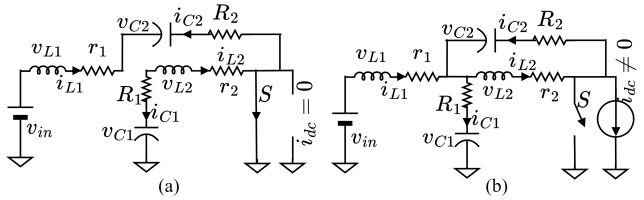

Fig. 3. Equivalent circuit of DC side (a) Under shoot-through, and (b) Under non-shoot-through conditions.

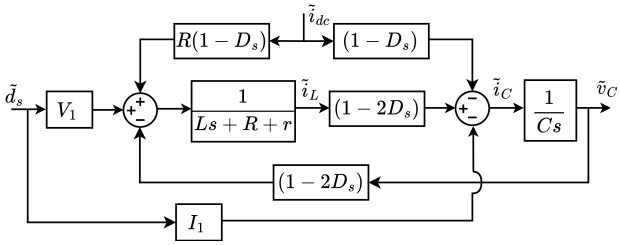

Fig. 4. DC side model block diagram of qZSI.

B. DC Side Modeling

For DC side modeling, the three-phase inverter bridge and the AC load are represented as a single switch and a current source connected in parallel [9]. Fig. 3(a) and Fig. 3(b) represent the shoot-through and non-shoot-through states of DC side qZSI. The model is developed by state-space averaging technique during shoot-through and non-shoot-through intervals. For simplification, assumption are taken as $C = C_1 = C_2, L = L_1 = L_2$, inductor resistance $r = r_1 = r_2$, and series resistance of capacitor $R = R_1 = R_2$. The shoot-through duty cycle is define as $D_s = T_0/T_s$,where T_0 and T_s are shoot-through interval and time period respectively. The averaged state-space model for the DC side of qZSI is given by (6), (7), (8) and (9).

$$L\frac{\partial I_{L1}}{\partial t} = -(r+R)I_{L1} - (1-D_s)V_{C1} + D_sV_{C2} + V_{in} + R(1-D_s)I_{dc} \tag{6}$$

$$L\frac{\partial I_{L2}}{\partial t} = -(r+R)I_{L2} + D_sV_{C1} - (1-D_s)V_{C2} + R(1-D_s)I_{dc} \tag{7}$$

$$C\frac{\partial V_{C1}}{\partial t} = (1-D_s)I_{L1} - D_sI_{L2} - (1-D_s)I_{dc} \tag{8}$$

$$C\frac{\partial V_{C2}}{\partial t} = -D_sI_{L1} + (1-D_s)I_{L2} - (1-D_s)I_{dc} \tag{9}$$

where I_{L1} and I_{L2} are inductor currents, V_{C1} and V_{C2} are capacitor voltages, V_{in} and I_{dc} are input dc voltage and equivalent DC side three-phase bridge current of impedance network respectively.

Now for small-signal model, perturbations $\tilde{i}_{L1}$, $\tilde{i}_{L2}$, $\tilde{d}_s$, $\tilde{v}_{C1}$, $\tilde{v}_{C2}$, and $\tilde{i}_{dc}$ are included in I_{L1}, I_{L2}, D_s, V_{C1}, V_{C2}, and I_{dc} respectively. The obtained small-signal model for the DC side of qZSI is shown by (10), (11), (12) and (13).

$$L\frac{\partial \tilde{i}_{L1}}{\partial t} = -(r+R)\tilde{i}_{L1} - (1-D_s)\tilde{v}_{C1} + D_s\tilde{v}_{C2} + R(1-D_s)\tilde{i}_{dc} + V_{11}\tilde{d}_s \tag{10}$$

$$L\frac{\partial \tilde{i}_{L2}}{\partial t} = -(r+R)\tilde{i}_{L2} + D_s\tilde{v}_{C1} - (1-D_s)\tilde{v}_{C2} + R(1-D_s)\tilde{i}_{dc} + V_{11}\tilde{d}_s \tag{11}$$

$$C\frac{\partial \tilde{v}_{C1}}{\partial t} = (1-D_s)\tilde{i}_{L1} - D_s\tilde{i}_{L2} - (1-D_s)\tilde{i}_{dc} - I_{11}\tilde{d}_s \tag{12}$$

$$C\frac{\partial \tilde{v}_{C2}}{\partial t} = -D_s\tilde{i}_{L1} + (1-D_s)\tilde{i}_{L2} - (1-D_s)\tilde{i}_{dc} - I_{11}\tilde{d}_s \tag{13}$$

where $V_{11} = V_{C1} + V_{C2} - RI_{dc}$ and $I_{11} = I_{L1} + I_{L2} - I_{dc}$. Further for simplification assumption is taken as $I_L = I_{L1} = I_{L2}$ and $V_C = V_{C1} = V_{C2}$. Applying the assumptions on (10), (11), (12) and (13), the equations are reduced as (14) and (15).

$$L\frac{\partial \tilde{i}_L}{\partial t} = -(r+R)\tilde{i}_L - (1-2D_s)\tilde{v}_C + R(1-D_s)\tilde{i}_{dc} + V_1\tilde{d}_s \tag{14}$$

$$C\frac{\partial \tilde{v}_C}{\partial t} = (1-2D_s)\tilde{i}_L - (1-D_s)\tilde{i}_{dc} - I_1\tilde{d}_s \tag{15}$$

where $V_1 = 2V_C - RI_{dc}$ and $I_1 = 2I_L - I_{dc}$. Using (14) and (15), the DC side model in the continuous domain of qZSI is developed by applying the Laplace transform, shown in Fig. 4. The transfer function for $\tilde{i}_L$ and $\tilde{v}_C$ is derived from Fig. 4 using Mason's rule.

$$G_i^{dc}(s) = \left.\frac{\tilde{i}_L}{\tilde{d}_s}\right|_{\tilde{i}_{dc}=0} = \frac{V_1Cs - I_1(1-2D_s)}{LCs^2 + C(r+R)s + (1-2D_s)^2} \tag{16}$$

$$G_c^{dc}(s) = \left.\frac{\tilde{v}_C}{\tilde{i}_C}\right|_{\tilde{i}_{dc}=0} = \frac{1}{Cs} \tag{17}$$

The steady-state values of capacitor voltages (18) and (19) are obtained by taking the average voltage across the inductor equal to zero. The detailed derivation is mentioned [5], [17]. The peak value of the DC-link voltage is shown by (20), and B as a voltage boost factor.

$$V_{C1} = \frac{1-D_s}{1-2D_s}V_{in} \tag{18}$$

$$V_{C2} = \frac{D_s}{1-2D_s}V_{in} \tag{19}$$

$$\hat{V}_{dc} = V_{C1} + V_{C2} = \frac{1}{1-2D_s}V_{in} = BV_{in} \tag{20}$$

Notice that the three-phase bridge output under steady-state, i.e., peak AC voltage (phase to neutral), can be written as (21).

$$V_{peak}(LN) = \frac{1}{2}\cdot\hat{V}_{dc}\cdot M = \frac{1}{2}\cdot\frac{V_{in}}{1-2D_s}\cdot M \tag{21}$$

where M is the modulation index. For simple-boost PWM technique, modulation and shoot-through duty cycle have inequality relations as (22) [18], [19].

$$M \le (1-D_s) \tag{22}$$

Hence from (20), (21), and (22), it is analyzed that the DC-link voltage and AC output can be controlled using shoot-through duty cycle and modulation index.

III. Controller Design for qZSI

The AC side and DC side controllers are designed separately. All the system parameters used in the control design are shown in Table I. For the feedback control loop, voltage and current sensors are used to reduce the system voltage to the controller signal level voltage. Along with sensors, LPF are used to filter out the noise that occurs due to PCB layouts and EMI interference. Hence the generalized transfer function for the AC current and voltage sensor, and DC current and voltage sensor along with LPF is shown by (23), (24), (25), and (26).

$$G_{is}^{ac}(s) = \frac{K_{is}^{ac}}{T_{is}^{ac} \cdot s + 1} \tag{23}$$

$$G_{vs}^{ac}(s) = \frac{K_{vs}^{ac}}{T_{vs}^{ac} \cdot s + 1} \tag{24}$$

$$G_{is}^{dc}(s) = \frac{K_{is}^{dc}}{T_{is}^{dc} \cdot s + 1} \tag{25}$$

$$G_{vs}^{dc}(s) = \frac{K_{vs}^{dc}}{T_{vs}^{dc} \cdot s + 1} \tag{26}$$

where K_{is}^{ac}, T_{is}^{ac}, K_{vs}^{ac} and T_{vs}^{ac} are AC current sensor gain, AC current sensor time constant, AC voltage sensor gain, AC voltage sensor time constant respectively, and K_{is}^{dc}, T_{is}^{dc}, K_{vs}^{dc} and T_{vs}^{dc} are DC current sensor gain, DC current sensor time constant, DC voltage sensor gain, DC voltage sensor time constant respectively.

In addition, the digital controller implements one sample period computational delay. Hence the one sample unit delay is also added while designing the AC and DC side controllers.

TABLE I
System Parameters

Parameter	Value	Parameter	Value
R_1, R_2	0.47Ω	R_f	4.6875Ω
C_1, C_2	$560\mu F$	C_f	$2.5\mu F$
L_1, L_2	$500\mu H$	L_f	$14\mu H$
r_1, r_2	0.03Ω	f_0	50Hz
V_{in}	$70V$ to $110V$	f_s	10kHz
$V_{base}(LL)$	$415V$	T_{vs}^{ac}, T_{is}^{ac}	$0.001sec$
S_{base}	$3kVA$	T_{vs}^{dc},T_{is}^{dc}	$0.006sec$
$V_{base}(DC)$	$180V$	K_{vs}^{ac}	0.00295
m_p	$0.5pu/sec$	K_{vs}^{dc}	0.00555
m_q	0.05	K_{is}^{ac}	0.1694
T_f	$0.2sec$	K_{is}^{dc}	0.06
T_{sp}	$1msec$	T_{sdc}	$1msec$
T_{sac}	$0.1msec$	T	$3ph, 3kVA$
			$60/415V, \Delta/Y$

A. AC Side Controller Design

Now to design the controller in the discrete domain, the discretization is performed on the AC side of the qZSI. Fig. 5 shows the discrete model of the AC side of the qZSI along the multi-loop control method. The inner control loop is a current control, whereas the outer control loop is a voltage control. A proportional controller is used in the inner control loop to respond faster and have no additional phase delay [9]. The outer control loop uses the PR controller to provide a stable three-phase balance voltage. Using the PR controller provides an advantage of zero study state error [11].

The zero-order hold (ZOH) transformation is used to discretize the $G_{ix}^{ac}(s)$ and $G_{PR}(s)$ and tustin method for discretizing the G_{cx}^{ac}, $G_{is}^{ac}(s)$ and $G_{vs}^{ac}(s)$. The reason for using ZOH for the forward path is to include the sampler and ZOH delay, whereas in the capacitor voltage and feedback path Tustin method is used, as it has no additional phase delay [20]. The unit delay is also added in the forward path as a one-sample computational delay is present in the digital implementation of the controller [21]. The AC side is discretized with a T_{sac} sample time. Now the following steps are performed to design the inner and outer loop controller.

Step 1: From Fig. 5, the open loop gain of the inner current control loop can be derived as (27)

$$T_i^{ac}(z) = K_{ip}^{ac} \cdot z^{-1} \cdot G_{ix}^{ac}(z) \cdot G_{is}^{ac}(z) \tag{27}$$

in which

$$G_{ix}^{ac}(z) = Z_{zoh}\left[\frac{V_{dc}}{2} \cdot N \cdot \frac{C_f s}{L_f C_f s^2 + R_f C_f s + 1}\right] \tag{28}$$

$$G_{is}^{ac}(z) = \frac{K_{is}^{ac}}{T_{is}^{ac} \cdot \frac{2}{T_{sac}} \frac{1-z^{-1}}{1+z^{-1}} + 1} = \frac{Y(z)}{X(z)} \tag{29}$$

where K_{ip}^{ac}, (28), (29), $Y(z)$, and $X(z)$ represent AC side proportional current controller, discrete current transfer function, discrete current sensor gain and LPF transfer function, sensor output in Z domain and sensor input in Z domain, respectively. To define the LPF parameters, (29) is transformed (using inverse Z-transform) in the form of discrete time polynomial equation as (30).

$$y[n] = K_1 \cdot x[n] + x[n-1] - K_2 \cdot y[n-1] \tag{30}$$

where $K_1 = T_{sac}/(T_{sac}+2\cdot T_{is}^{ac})$ and $K_2 = (T_{sac}-2\cdot T_{is}^{ac})/(T_{sac}+2\cdot T_{is}^{ac})$ are the parameter of the LPF. In the subsequent section, the LPF parameter is defined

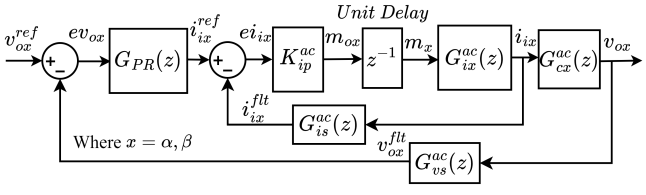

Fig. 5. Discrete AC side control block diagram using multi-loop control in $\alpha\beta$ reference frame.

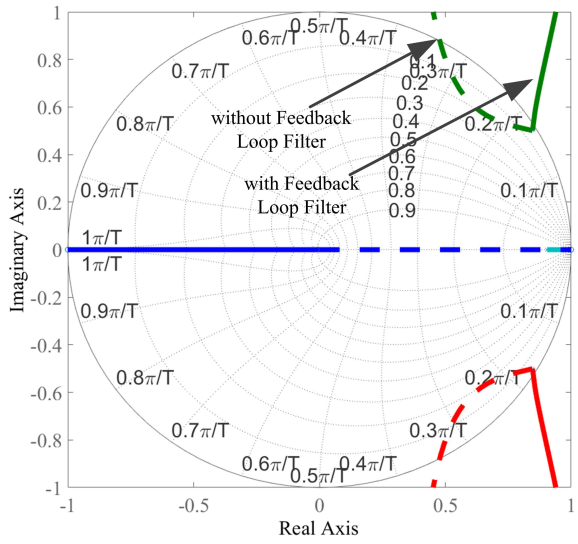

Fig. 6. AC-side inner current loop root loci.

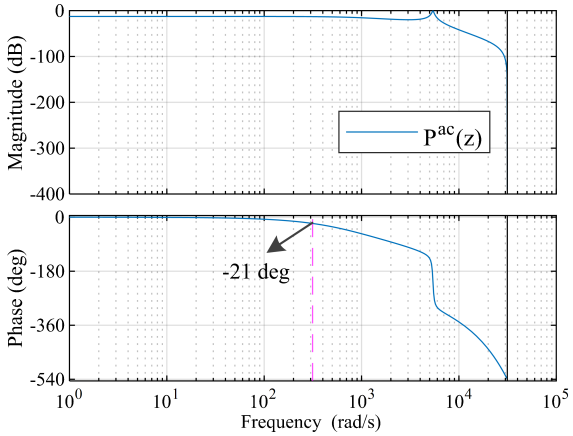

Fig. 7. Frequency response of AC side open loop gain of voltage loop with unity controller.

similarly as (30). Now, the root loci method is used to define the proportional gain of the current controller. The characteristic equation of the inner current control loop is shown as (31).

$$1 + T_i^{ac}(z) = 0 \tag{31}$$

Fig. 6 shows the root loci of (31) with and without the AC current sensor filter ($G_{is}^{ac}(z)$). From Fig. 6, it is clear that the filter causes stability issues in the system as it shifts the root loci outside the unit circle as the gain of the system increases. Now the gain of the current controller is selected such that the root lies within the unit circle to ensure stability. The K_{ip}^{ac} is set to 0.13, with the damping ratio of complex poles equal to 0.0209.

Step 2: From Fig. 5, the open loop gain of the voltage loop can be derived as (32).

$$T_v^{ac}(z) = G_{PR}(z) \cdot GCL_{ix}^{ac}(z) \cdot G_{cx}^{ac}(z) \cdot G_{vs}^{ac}(z) \tag{32}$$

in which

$$G_{PR}(z) = Z_{zoh}\left[K_{vp}^{ac} + \frac{K_r^{ac}(s \cdot cos\theta_c - \omega_1 \cdot sin\theta_c)}{s^2 + \omega_c \cdot s + \omega_1^2}\right] \tag{33}$$

$$GCL_{ix}^{ac}(z) = \frac{K_{ip}^{ac} z^{-1} G_{ix}^{ac}(z)}{1 + K_{ip}^{ac} z^{-1} G_{ix}^{ac}(z) G_{is}^{ac}(z)} \tag{34}$$

$$G_{cx}^{ac}(z) = \frac{1}{C_f \cdot \frac{2}{T_{sac}} \frac{1-z^{-1}}{1+z^{-1}}} \tag{35}$$

$$G_{vs}^{ac}(z) = \frac{K_{vs}^{ac}}{T_{vs}^{ac} \cdot \frac{2}{T_{sac}} \frac{1-z^{-1}}{1+z^{-1}} + 1} \tag{36}$$

where (33), (34), (35) and (36) represent the discrete phase compensated PR controller, inner current controller closed loop, capacitor, and discrete sensor transfer function, respectively. Now the PR controller parameters are designed in the subsequent steps.

Step 3: The ω_1 in (33) is the system frequency i.e. 100π rad/s. Generally, the resonant bandwidth ω_c is adjusted between 2 and 10 rad/s to deal with frequency deviation. The resonant bandwidth helps achieve the frequency deviation that occurred due to $P-f$ droop control. Here ω_c is set to 3.1416 rad/sec, considering 1% deviation in system frequency [22].

Step 4: As shown in Fig. 5, the total phase delay caused in the voltage control loop is the sum of inner current loop phase delay, capacitor output, and sensor LPF filter. The frequency response of (37) is analyzed to obtain the total phase delay [23]. Equation (37) is obtained from (32) with unity controller in place of PR controller.

$$P^{ac}(z) = GCL_{ix}^{ac}(z) \cdot G_{cx}^{ac}(z) \cdot G_{vs}^{ac}(z) \tag{37}$$

Fig. 7 shows the frequency response of (37), and the phase delay is compensated accordingly. The phase delay at $\omega_1 = 100\pi\ rad/s$ is equal to $-21°$. In addition, as the $\Delta - Y$ transformer is used AC side, the phase shift of $30°$ occurs between primary and secondary. Hence the phase compensation angle $\theta_c = 21° - 30° = -9°$ for the PR controller.

Step 5: For defining the resonant gain of the PR controller, the root locus method is used. The outer loop system's characteristic equation with the PR controller's resonant part is shown as (38).

$$1 + T_v^{ac}(z) = 0, \quad where\ K_{vp}^{ac} = 0 \tag{38}$$

Fig. 8 shows the root loci of (38) with the resonant part of the PR controller along with values defined in obtained in previous steps. From Fig. 8, it is clear that K_r^{ac} value should be selected such that the poles should be within the unit circle to ensure the stability of the system. Whereas the value of K_r^{ac} should not be too less which makes the system response slow. The K_r^{ac} is set to 2600, and the damping ratio of

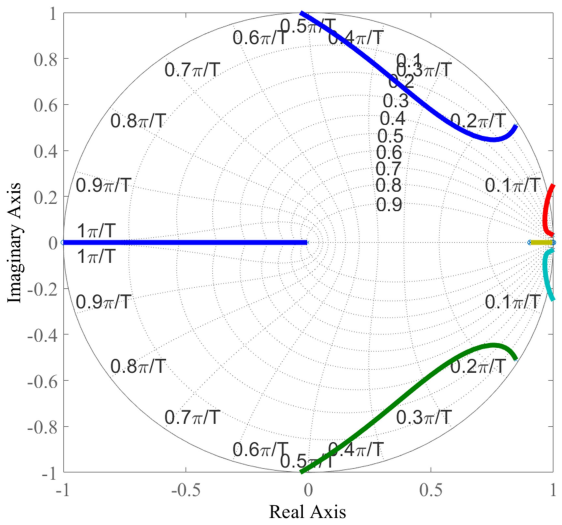

Fig. 8. AC-side outer voltage loop root loci.

the two pairs of complex poles is equal to 0.422 and 0.0297.

Step 6: For defining the K_{vp}^{ac} the frequency response of (32) is analyzed along with the values defined in previous steps. Fig. 9 shows the frequency response of (32). The K_{vp}^{ac} is selected such that the cross-over frequency is increased while having sufficient gain margin (GM) and phase margin(PM). The K_{vp}^{ac} is set equal to 0.2 at which the system has $GM = 19.5dB$, $PM = 46.3°$, and a cutoff frequency of 653 rad/s.

To obtain the controller parameter, heuristic approaches [24], [25] can be used, which are computationally intensive. This paper uses the classical approach for tuning the controller parameter with GM and PM. The flowchart is shown in Fig. 10 for controller parameter tuning.

Further, to emulate the synchronous machine behavior, the droop control is implemented in the AC side of qZSI. The relation between the real power to frequency $(P - f)$ and reactive power to voltage $(Q - V)$ as per droop in shown by

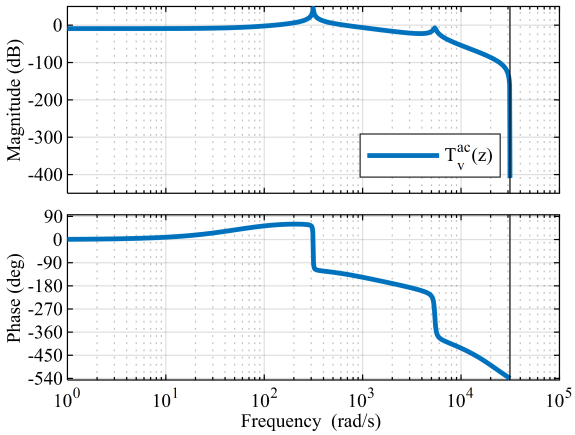

Fig. 9. Frequency response of AC side open loop gain of voltage loop.

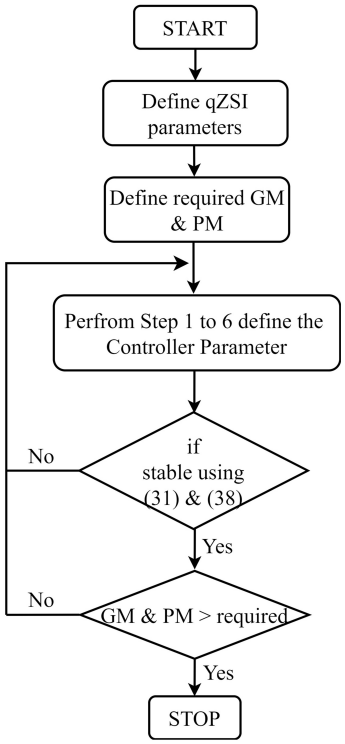

Fig. 10. Flowchart for controller parameter tuning.

(39), and (40) respectively [26], [27].

$$f = f_0 - m_p(P - P_0) \tag{39}$$

$$V = V_0 - m_q(Q - Q_0) \tag{40}$$

where f_0, V_0, P_0, Q_0, m_p, and m_q are nominal frequency, nominal voltage, active power at nominal frequency, reactive power at nominal voltage, real power droop gain, and reactive power droop gain respectively. P and Q represent the average active and reactive power and are calculated as per (41) and (42), respectively.

$$P = \frac{1}{T_f \cdot s + 1} \cdot p \tag{41}$$

$$Q = \frac{1}{T_f \cdot s + 1} \cdot q \tag{42}$$

where T_f is the time constant of the LPF used to filter the calculated instantaneous power, p and q are instantaneous active and reactive power, and are calculated in $\alpha\beta$ stationary reference frame shown by (43) and (44).

$$p = v_{o\alpha} i_{o\alpha} + v_{o\beta} i_{o\beta} \tag{43}$$

$$q = v_{o\beta} i_{o\alpha} - v_{o\alpha} i_{o\beta} \tag{44}$$

The discretization of (41) and (42) is performed using Tustin method with sample time T_{sp}. Now the reference generated from droop equations (39) and (40) is used as controller reference for generating three-phase AC voltage in qZSI.

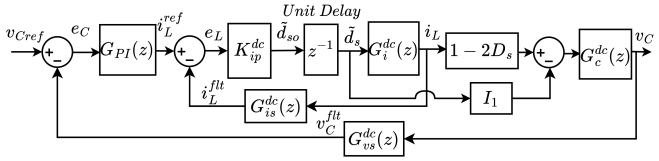

Fig. 11. Discrete DC-side control block diagram using multi-loop control.

B. DC Side Controller Design

To control the DC-link voltage, the feedback signal in a voltage control loop needs to be a DC-link voltage. But as the dc-link voltage is pulsating in nature due to shoot-through, the DC-link voltage can not be taken as a feedback signal. Hence to control the DC-link voltage, the indirect method is used. This method takes the capacitor voltage v_{C1} as a feedback signal. The reference of the capacitor voltage is shown in (45) and is obtained by solving the (18) and (21).

$$v_{Cref} = \frac{(v_{in} + V_{dcref})}{2} \tag{45}$$

To develop the digital controller, discretization is performed DC side of qZSI. Fig. 11 shows the discrete model of the DC side of qZSI along with multi-loop control. The inner loop is the current control of the inductor, and the outer loop is the voltage control of the capacitor. A proportional controller is used in the inner control loop, whereas PI controller is used in the outer loop control.

The ZOH transformation is used to discretize (16), whereas the Tustin method is used to discretize (17), (25), (26) and PI controller. The reason for using ZOH to discretize the (16) is to include the signal propagation and ADC sampler delay. The Tustin method is used for (17), (25), (26), and PI controller, as it has no additional phase delay. In addition, a unit delay is also added in the forward path to compensate for the one-sample digital delay. The DC side is discretized with T_{sdc} sample time.

From Fig. 11, the open-loop gain of the current loop in the DC side of qZSI can be derived as (46)

$$T_i^{dc}(z) = K_{ip}^{dc} \cdot z^{-1} \cdot G_i^{dc}(z) \cdot G_{is}^{dc}(z) \tag{46}$$

in which

$$G_i^{dc}(z) = Z_{zoh}\left[\frac{V_1 Cs - I_1(1-2D_s)}{LCs^2 + C(r+R)s + (1-2D_s)^2}\right] \tag{47}$$

$$G_{is}^{dc}(z) = \frac{K_{is}^{dc}}{T_{is}^{dc} \cdot \frac{2}{T_{sdc}} \frac{1-z^{-1}}{1+z^{-1}} + 1} \tag{48}$$

where (47), (48), and K_{ip}^{dc} represent the discrete DC side inductor current transfer function, discrete sensor transfer function, and inner current proportional controller on the DC side, respectively. Similarly, from Fig. 11, the open loop gain of the voltage loop in the DC side of qZSI can be derived as (49).

$$T_v^{dc}(z) = G_{PI}(z) \cdot K_{ip}^{dc} \cdot z^{-1} \cdot \frac{G_i^{dc}(z)(1-2D_s) - I_1}{Cs(1 + K_{ip}^{dc} z^{-1} G_i^{dc}(z) G_{is}^{dc}(z))} \cdot G_{vs}^{dc}(z) \tag{49}$$

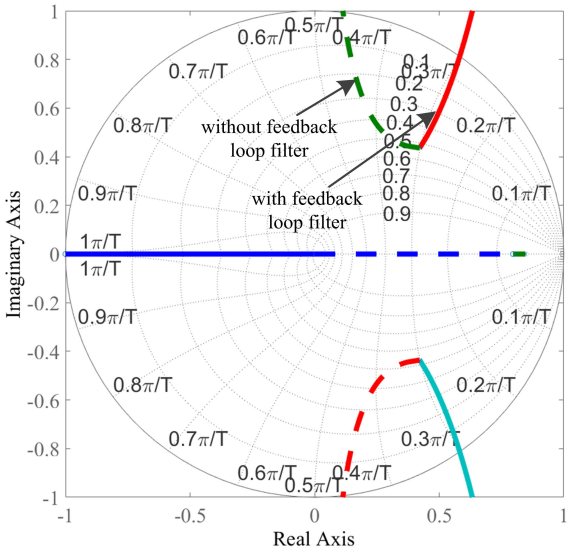

Fig. 12. DC side inner current loop root loci.

in which

$$G_{PI}(z) = K_{vp}^{dc} + K_{vi}^{dc} \cdot \frac{T_{sdc}}{2} \frac{1+z^{-1}}{1-z^{-1}} \tag{50}$$

$$G_{vs}^{dc}(z) = \frac{K_{vs}^{dc}}{T_{vs}^{dc} \cdot \frac{2}{T_{sdc}} \frac{1-z^{-1}}{1+z^{-1}} + 1} \tag{51}$$

where (50) and (51) represent the discrete PI controller and discrete sensor transfer function, respectively. Now to define the K_{ip}^{dc}, K_{vp}^{dc} and K_{vi}^{dc} values of the inner and outer loop controller, the following steps are performed.

Step 1: The Root loci method is used to define the K_{ip}^{dc}. The characteristic equation for the inner current loop is shown as (52)

$$1 + T_i^{dc}(z) = 0 \tag{52}$$

Fig. 12 shows the root loci of (52) with and without the DC current sensor filter $(G_{is}^{dc}(z))$. It is clear from the root loci that the filter causes the stability issue as it shifts the root loci outside the unit circle as the system gain increases. Now the current controller gain is selected, so the root loci lie with the unit circle to ensure stability. The K_{ip}^{dc} is set to 0.0402, with the damping ratio of complex poles equal to 0.394.

Step 2: Now for defining the K_i^{dc}, the again root loci method is used. The characteristic equation of the DC side outer loop with an integral part of the PI controller is shown as (53).

$$1 + T_v^{dc}(z) = 0, \quad where\ K_{vp}^{dc} = 0 \tag{53}$$

Fig. 13 shows the root loci of (53). From Fig. 13, it is clear that K_{vi}^{dc} value should be selected such that the poles should be within the unit circle to ensure the stability of the system. The K_{vi}^{dc} value should not be too low, making the system response too slow. Another point is that the system response should be slower than the AC side controller. The K_{vi}^{dc} is set

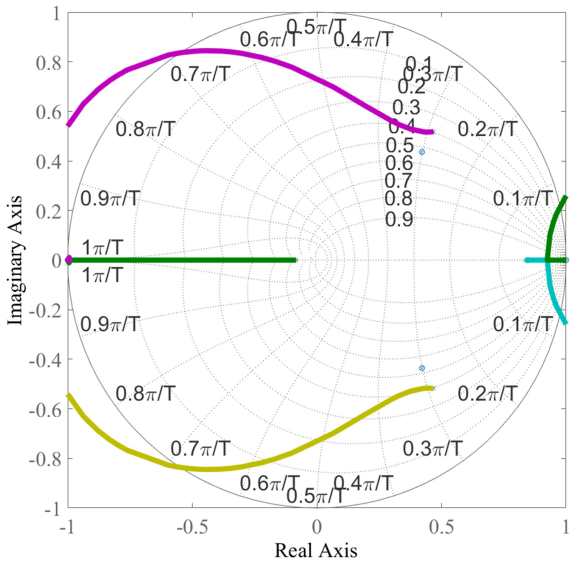

Fig. 13. DC-side outer voltage loop root loci.

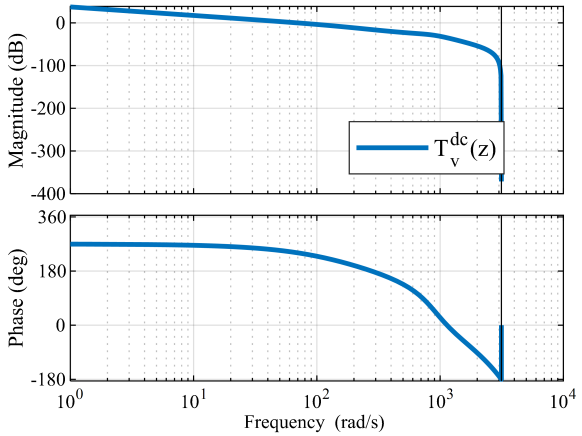

Fig. 14. Frequency response of DC side open loop gain of voltage loop.

as equal to 1180 with the GM 17 dB and PM 67.8°. The phase crossover and gain crossover frequencies are 221 rad/s and 45.3 rad/s.

Step 3: To further speed-up the response the K_{vp}^{dc} is set to 1.0 with GM 15.6 dB and PM 60.8° at phase crossover 278 rad/s and gain crossover 69.5 rad/s. The frequency response of (49) including K_{vp}^{dc} is shown in Fig. 14. Like the AC side controller parameters tuning shown in Fig. 10, the DC side controller parameters are also tuned by using (52) and (53).

IV. Controller Implementation in DSP

The overall control strategy for the qZSI is depicted in Fig. 15. The sine pulse width modulation (SPWM) is generated using the AC controller output. In contrast, the DC side controller output enhances the DC link voltage through shoot-through generation. Typically, shoot-through is produced by combining the AC and DC side controller outputs using "OR" gate integrated circuits (ICs). In this paper, the shoot-through is generated using two controller timers and programmatically

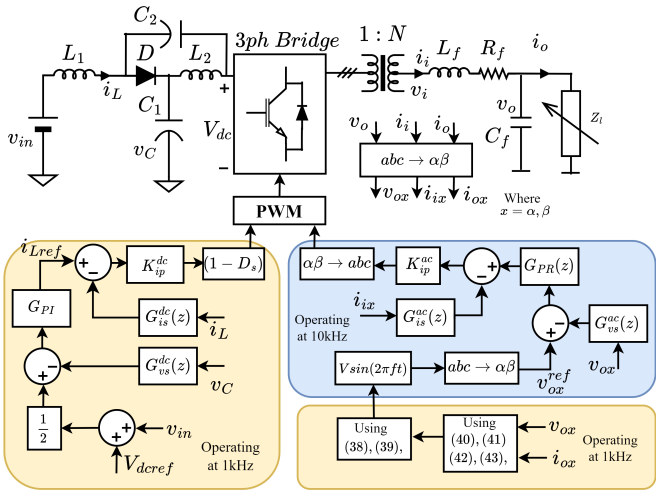

Fig. 15. Overall proposed control strategy for qZSI .

controlling the digital output pins. In two timer method, one timer is used for SPWM generation, whereas the second timer is used for shoot-through generation. Additionally, a dead band (DB) is introduced between the modulation index and the shoot-through duty cycle. The steps involved in implementing the control strategy in DSP controller is shown by pseudocode (Algorithm 1). The algorithm has three functions. First is the main function used to enable and disable PWM pins. The second function is interrupt service routine 1 (ISR1), which calculates the modulation index. The third function is interrupt service routine 2 (ISR2), which calculates the shoot-through duty cycle, the reference frequency, and voltage from droop control.

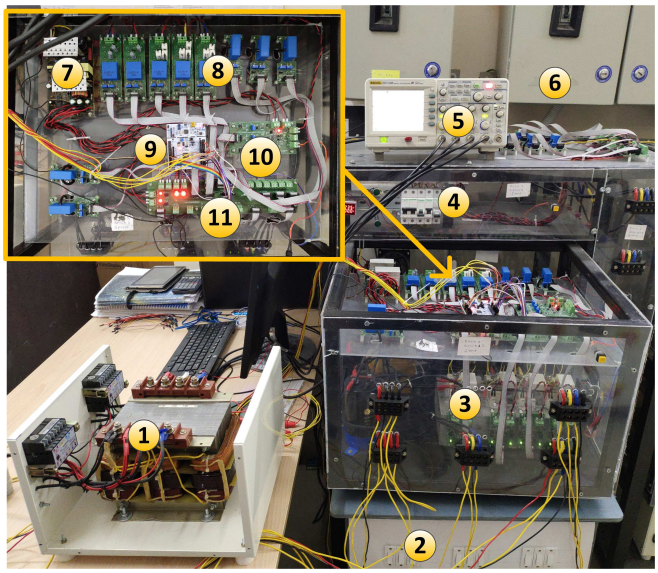

Fig. 16. Hardware setup: 1) Transformer. 2) Load. 3) 3ph qZSI stack. 4) Rack power supply. 5) Oscilloscope. 6) Supply. 7) Housekeeping power supply. 8) Current and voltage sensors. 9) Controller - STM32F446RE. 10) Trip and over-current circuit. 11) Power and signal routing board.

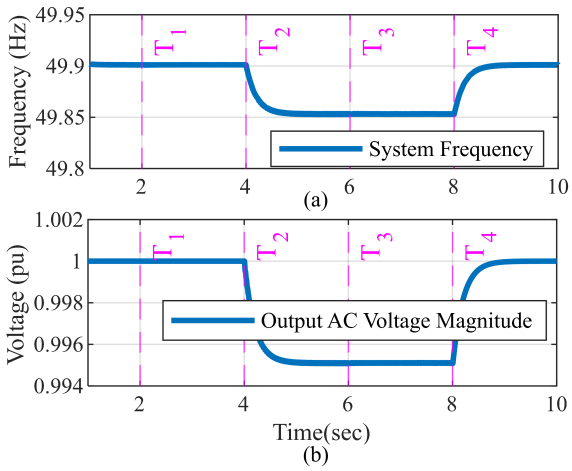

Fig. 19. Simulation result (a) System frequency and (b) Output AC voltage magnitude.

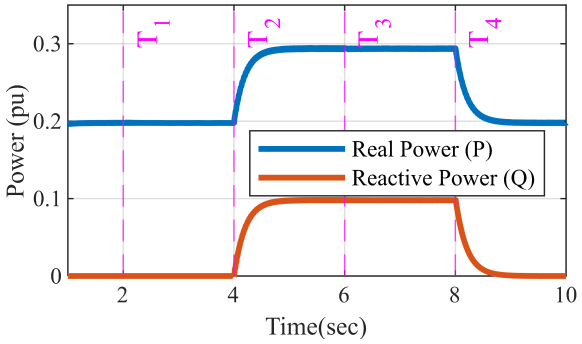

Fig. 20. Simulation Result for active and reactive power variations.

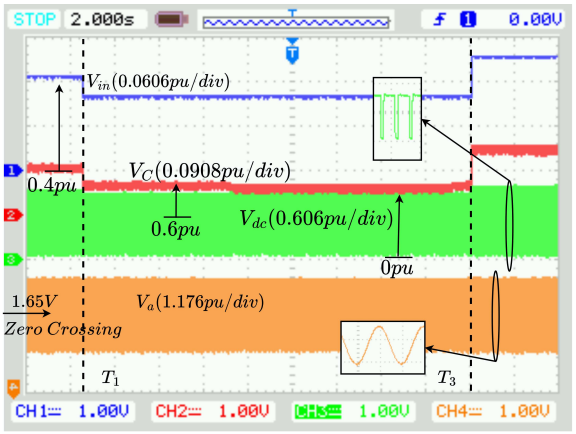

Fig. 21. Experimental result for input DC voltage, capacitor, DC-link voltage, and AC output phase voltage.

A. Before time T_1

Before time T_1, the input DC voltage is 0.527 pu as shown in Fig. 18(a) and Fig. 21. The capacitor reference voltage is set to 0.7638 pu as per (45). Fig. 18(b) and Fig. 21 shows the tracked capacitor voltage to 0.75 pu under simulation and experimentation, respectively. Simultaneously the DC-link voltage is boosted up to 1 pu. The DC-link voltage is pulsating in nature with zero voltage under shoot-through conditions and

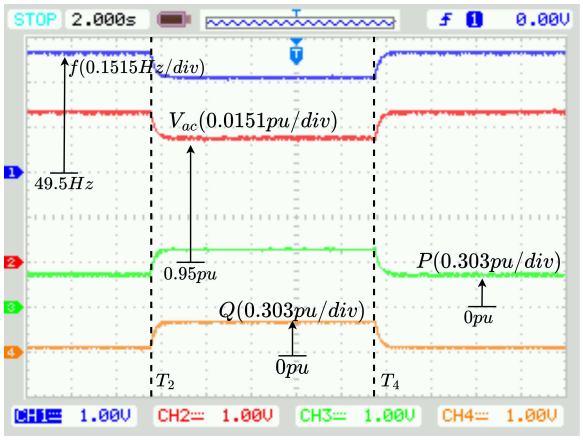

Fig. 22. Experimental result system frequency, ac voltage magnitude, active and reactive power.

1 pu under normal switching conditions shown in Fig. 21.

B. At time T_1 instant

At this instant, the input DC voltage is changed from 0.527 pu to 0.5 pu. The reference of the capacitor voltage is changed from 0.7638 pu to 0.75 pu as per (45). The tracked capacitor voltage and the boosted DC-link voltage are shown in Fig. 18(b), Fig. 18(c) and Fig. 21. Meanwhile, there is no change in system frequency, output AC voltage, and power, as shown in Fig. 19, Fig. 20 and Fig. 22.

C. At time T_2 instant

At this instant, under simulation, the active power load increases from 0.2 pu to 0.3 pu, and the reactive power load from 0 pu to 0.1 pu. Due to the increase in load power, the system frequency and AC voltage are reduced as per droop equations (39) and (40). Meanwhile, the DC capacitor voltage remains unchanged.

D. At time T_3 instant

The load power remains unchanged in this time interval, whereas the input DC voltage is changed from 0.5 pu is 0.555 pu. As per equation (45), the reference of the capacitor voltage is set to 0.777 pu. The DC-link voltage is maintained at 1 pu. The system frequency and AC voltage remain unchanged.

E. At time T_4 instant

The input DC voltage remains unchanged at this instant, whereas the load is decreased. Due to the decrease in load power, the system frequency and AC voltage are increased as per (39) and (40). Meanwhile, the capacitor voltage remains unchanged, and the DC-link voltage is maintained at 1 pu.

Furthermore, a comparison between the proposed control scheme and existing control schemes presented in [9], [13]–[15], [28] is provided in Table II. The analysis shows that the proposed control scheme offers effective implementation in low-cost controllers with reduced complexity.

TABLE II
COMPARISON BETWEEN THE PROPOSED AND EXISTING TECHNOLOGIES

Attribute	[9]	[13]	[28]	[14]	[15]	Proposed
Control method (AC side)	ML - OL(P) & IL(P)	SL - PR	SL - PR	SL - MPC	SL - MPCVV	ML - OL(PR) & IL(P)
Control method (DC side)	SL - PI	SL - PI	SL - PI	SL - MPC	SL - MPCVV	ML - OL(PI) & IL(P)
Controller parameter tuning	×	×	×	×	×	✓
Droop control implementation	×	×	✓	×	×	✓
Discretization while controller design	×	×	×	×	×	✓
LPF consideration	×	×	×	×	×	✓
Controller	LF2407	MicroLab	MicroLab	F28335	F28335	F446RE
Controller cost	Moderate	High	High	Moderate	Moderate	Low
Shoot-through implementation by	'OR' gate IC	Fully SW	ND	Fully SW	Fully SW	SW & Timer
Complexity	Moderate	Moderate	Moderate	High	High	Less
Controller computation burden	High	High	Less	High	High	Less

ML: Multi loop, OL(X): Outer loop with X controller type, IL(X): Inner loop with X controller type, SL: Single loop, ND: Not defined, ✓: Yes, ×: No, SW: Software.

VI. CONCLUSION

In this paper, a digital controller design for the qZSI using multi-loop control on the AC and DC sides is proposed. A simplified qZSI model is discretized to design the controller for AC and DC sides. The stability issue caused by the sensor gain and LPF used in the feedback is addressed in designing the controller. On the AC side, a P controller is used for inner current control and a PR controller for outer voltage control. On the DC side, a P controller is used for the inner inductor current control and a PI controller for the outer capacitor voltage control. Shoot-through pulses are generated using controller timers and programmatically controlled digital output pins. The AC controller is developed in the stationary reference frame to reduce the computational burden.

The control scheme also incorporates droop control to emulate synchronous generator behavior and a dead band between the shoot-through duty cycle and modulation index for proper operation. Time domain simulations and experiments validate the proposed control scheme under different operating conditions. The proposed control scheme has the advantage of cost-effectiveness and reduced complexity.

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