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DC-DC Converter For Fuel Cell (Control Strategy, Voltage Curve, Optimization, Converter Type)

Current-fed Full-bridge Isolated DC-DC Converter With An Active Clamp Circuit For Fuel Cell Application

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Master Thesis

UiT The Arctic University of Norway

Abstract

This thesis presents the design, analysis the efficiency of a current-fed full-bridge isolated DC-DC converter with an active clamp circuit for a fuel cell in a marine application. Compared to the voltage-fed converters, current-fed converters have a higher voltage conversion ratio, lower input current ripple, and higher efficiency to meet the requirements of a fuel cell. Active-clamp circuit, in addition to absorbing the turn-off voltage spike across the switch, acts as a zero voltage transition auxiliary circuit resulting in zero voltage switching (ZVS) of the switches.

Detailed operation, analysis, design, and simulation for the converter are presented for a fuel cell with a voltage range of $800V$ to $1000V$. A fixed frequency two-loop average current control duty cycle modulation is designed to operate the converter for input voltage and load variation. The design procedure is illustrated by the state-space averaging technique. An experimental converter prototype rated at $20W$ (for an input voltage of $12V$ to $20V$) is redesigned, built, and tested in the laboratory to verify the designed method at higher rates.

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Introduction

Due to the technology development and environmental protection, some distributed energy resources, such as combustion engines, gas turbines, microturbines, photovoltaics, Fuel Cells (FC), and wind powers have emerged within the distribution system. A better way to realize the emerging potential of distributed generation and associated loads is as a subsystem called a microgrid. Microgrid distribution networks for integrating renewable energy resources can classify into AC or DC bus interconnection.

In AC networks, reactive power increases losses and reduces transmission capacity while this problem does not exist in DC networks. Depending on the application, DC grids offer great potential for energy savings. Aside from reducing CO_2 emission and financial costs, DC microgrids may provide the best solution for increasing the penetration of renewable energy sources in a distribution network and improving the system efficiency [1], [2].

A microgrid, as shown in Figure 1.1, is a system whose different alternative energy sources are connected to the main DC bus bar through power electronic interfacing circuits. In a DC microgrid, the power transfers from different generators and storage to the utility grid and AC or DC loads through the main bidirectional DC-AC or DC-DC converters. The backup diesel generator and the FC should provide the peak load and charge the storage units simultaneously, while the utility grid can maintain the voltage level of the DC bus and cover the required load demand if the DC microgrid fails [3].

Power electronic converters are utilized in microgrids to manage the flow of power and convert it into suitable DC or AC form as required. Different converter configurations, such as AC-DC rectifiers, DC-DC converters, and DC-
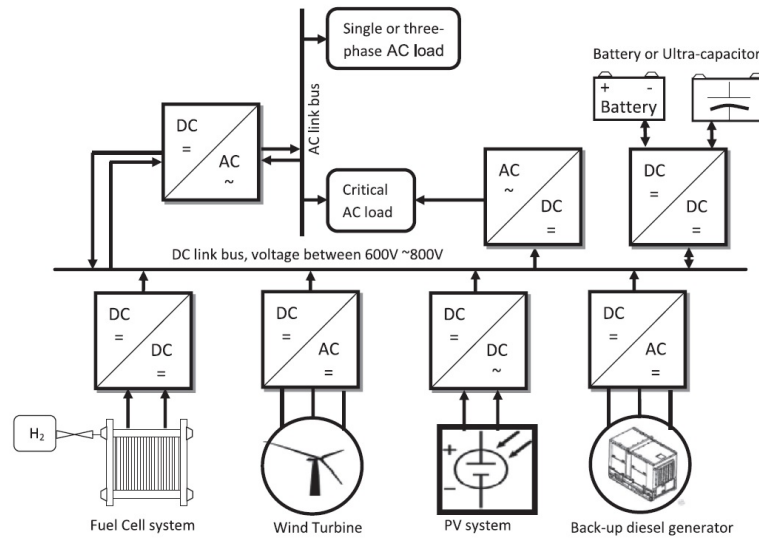
Figure 1.1: DC microgrid power system with resources and loads [3].

AC inverters, are necessary to take advantage of the microgrid, as shown in Figure 1.1. However, power electronic circuits are quite costly due to their complicated technology. They are the most common sources of harmonics (due to pulse width modulation technique), and they may increase the losses through the microgrid system, and cause low power quality for a microgrid bus and resources. Hence, the overall efficiency of the microgrid system depends on the efficiency of these converters and inverters. High-efficiency and low-cost converters are necessary to obtain a cost-effective solution.

A hydrogen-oxygen fuel cell is one of the most promising technologies to solve environmental concerns. Interest in FC systems arises not only because of their zero pollution emission but also because of their energy conversion efficiency, which can be higher than that of a conventional power plant [4]. Additionally, thermal energy generated as the by-product of FC can be used for heating. Since the power density of FC is higher than the renewable energies or even batteries, it can be widely used in the real world [4], [5].

This study aims to investigate high-efficiency power electronic converters for the interconnection of FC to the loads or a DC microgrid. For an appropriate selection for the power converters, the characteristic of the FC is first described and studied here.

Fuel Cell Characteristics:

Fuel cells convert the chemical energy from a fuel into electricity through a chemical reaction with oxygen or another oxidizing agent. The fuel for the FC is normally hydrogen or any other compound which may produce hydrogen [6].
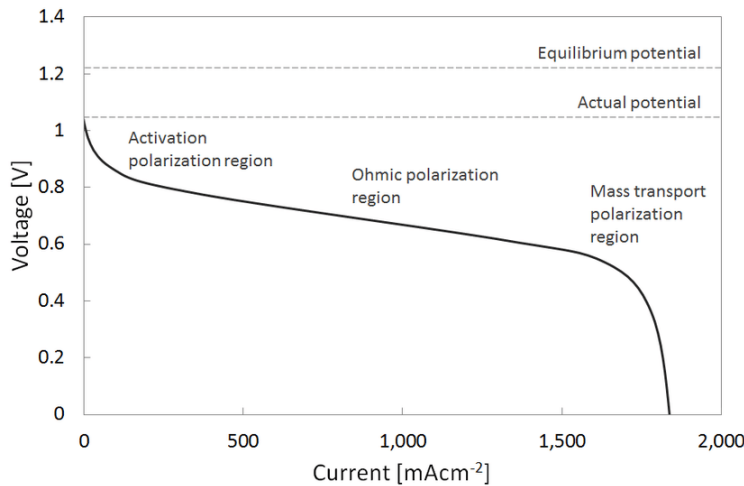
Figure 1.2: $V - I$ characteristic of FC [5].

There exists various fuel cells available for industrial use, although not all of them are available commercially. The FC characteristic differs from the renewable sources' characteristics. This characteristic has three regions of operation as shown in Figure 1.2. These regions are very important in deciding converter operating set point for maximum power extraction from the FC.

In the ohmic polarization region, voltage drops linearly with the current density [5]. This is because of the Ohmic contact which limits the output voltage. In the mass transport polarization region, the change in output voltage varies rapidly due to the gas exchange efficiency. At a low current level, the Ohmic loss becomes less significant, and the increase in output voltage is mainly due to the activity of the chemicals in the activation polarization region.

Since the voltage produced by each cell is around $0.6V_{DC}$ at full load, many cells need to be stacked to obtain a higher voltage. Besides low voltage at the output of stack, poor response to load variations, permitting reverse current flow, and presence of ripple current are other disadvantages associated with fuel cell [7].

Another issue with FC is its low isolation to ground resistance. This may create a path for common-mode noise and leakage current, which cuts down the performance of FC. If other AC generators exist as a backup in the system, this complex mix of AC and DC systems leads to many leakage current pathways and common-mode noise. Besides the efficiency of the system, safety is another problem needed to be considered in this matter. To overcome the above technical challenges and connect FC to the utility grid, a high step-up DC-DC converter with a high voltage conversion ratio (depending on the applications), low input current ripple, high efficiency, and isolation is required.

Selection Of A Converter:
The variety of topologies is presented mainly about DC-DC converters, which are difficult to design and control because they are directly connected to the FC at the first stage and need to overcome the disadvantages of the FC. Although they meet the general requirements of boost DC-DC converters, they are based on voltage-fed configuration and they have no dynamic verification with the actual FC characteristics [8], [9].

Compared with the other applications in the FC applications, voltage-fed converter configurations may not be optimal due to the severe ripple current characteristic of the FC. In order to handle the ripple current, an additional LC filter (with large electrolyte capacitance) across the FC stack is essentially required, resulting in an increase in the overall system size and manufacturing cost [10]. Furthermore, in a voltage-fed converter, as the boosting action is only performed by the transformer, a high winding ratio between the primary and secondary sides of the high-frequency transformer is necessary. It causes the snubber circuit to be enlarged to handle the surge at turn-off switching instants.

On the other hand, in a current-fed converter, using a boost inductor decreases the current ripple as well as the electrolyte capacitor. Another advantage of the current-fed converter configuration is active boosting action can be achieved with relatively a low winding ratio which means lower losses in the converter. Therefore, for the FC system, current-fed converters are a better choice than the voltage-fed ones. Several current-fed converters have been developed such as the current-fed push-pull, the current-fed resonant, current-fed half-bridge, current-fed full-bridge converter, etc.

A high-Frequency (HF) transformer can act as the electrical barrier between source and load and improve the low galvanic isolation of FC issues to a certain level. Moreover, a high frequency of operation reduces the number of turns of the transformer and thereby cuts down its size and core losses considerably.

The objective of this thesis is to present the analysis, design, and physical model of the current-fed full-bridge isolated DC-DC converter with a rectifier on the secondary side and study its efficiency. Current-fed converters suffer from severe voltage overshoots at turn-off due to the stored energy in the leakage inductor of the transformer. Adding the lossless snubber and clamp circuits can solve the inherent problem of the converter.

1.1   Objective

The main objective of this thesis is to investigate the efficiency of a current-fed full-bridge isolated DC-DC converter with an active clamp circuit that meets the requirements of an FC and generates a DC voltage link from an FC. The control method is needed to be presented and applied to the converter to have

a constant DC voltage link regardless of the ripple in FC current and voltage. Hence, the following objectives were set for the master thesis:

1) Investigating the operation and feasibility of the selected converter, HF transformer, and designed controller based on the assumptions and requirements.

2) Modeling and simulating the complete system in MATLAB R2021b and Simscape under various loads.

3) Analyzing the common-mode current through the system and some reduction methods.

4) Inspecting the efficiency of the system under various loads and frequencies, investigating ZVS and cause of losses to improve the system.

5) Building the converter and transformer in the laboratory with scaled values.

6) Studying the performance of the experimental model and analyzing the differences between the physical model and simulation.

1.2   Method

The first part of this thesis is the theory and preliminaries required to acknowledge the converter operation and functionality of auxiliary elements inside the circuit. Mode by mode, the operation of the converter is explained for one complete half cycle because the system is symmetric and two half-cycles are the same. Analyzing the operation of the converter leads to designing and calculating the converter's elements based on the requirements and assumptions. The controller method is introduced and required parameters are calculated with the help of small-signal analysis. The leakage current phenomenon's causes and effects are discussed, and some available reduction methods are studied. From here, simulations on MATLAB and Simscape are done to check the designed converter's behavior and its controller.

To confirm the accuracy of the used methods, a physical model is built in the laboratory. As the simulation was done for high voltage and current (assumptions), the whole system is redesigned and simulated with new assumptions for the experimental model. The transformer designing method is explained briefly and built in the laboratory. Also, its specializations' values such as resistances, leakage, and magnetizing inductances are measured and used in the simulation.

The converter is built by an Intelligent Power Module (IPM) is used as the switches of the primary side of the converter, a diode bridge as the secondary side rectifiers, HF transformer, and associated elements. Before connecting the controller to the converter, the converter is controlled manually to verify the results and clear faults and disorders. Then, the controller is added to the converter with the help of dSPACE 1202 (ControlDesk software and MicroLab-Box). The efficiency and losses of the system are analyzed under various loads and frequencies, and compared with the result of the simulation part. And

at the end, some suggestions are offered to improve the performance of the system.

1.3   Structure

Chapter2: In the first part, some of the most commonly used converter topologies are listed and their advantages and drawbacks are briefly explained. Theory and other preliminaries from the specialization project relevant to the thesis are summarized as well. This includes the design of a chosen converter, the design of a controller, and the analysis of power losses and leakage currents. Furthermore, the reduction method for leakage current is studied.

Chapter3: This chapter includes the simulation of the designed converter based on the theory in the last chapter. Also, the effect of the auxiliary clamp circuit is investigated. The controller's simulation is added to the converter and the performance of the system is analyzed on both MATLAB and Simscape.

Chapter4: In this chapter, first, redesigned converter and controller with scaled values for a physical experiment are introduced. The model is built by two IPM modules, a transformer, dSPACE equipment, and complementary elements. Then, the results of the built model are investigated and efficiency is analyzed to other possible assumptions in terms of frequency and load.

Chapter5: The final results are discussed for the converter and controller. Some improvements suggestion are offered for further work.

Chapter6: This chapter is the conclusion and gives an overview of the thesis.

/2

Converter Topologies, Operation and Design

A variety of topologies is presented about DC-DC converters, with two main categories, Voltage-Fed Convereter (VFC) and Curret-Fed Converter (CFC). In this chapter, first, some popular DC-DC converter for a Fuel Cell (FC) is briefly mentioned, then, the operation of the chosen converter is discussed and analyzed.

2.1 Converter Topologies

Voltage-fed bidirectional dual active bridge (DAB) DC-DC converter:
Voltage-fed DAB, shown in Figure 2.1, is one of the preferred topologies for its attractive advantages such as simple structure, high-power density, bidirectional power transfer capability, and ZVS in turn-on. However, For DAB, if the voltage conversion gain deviates away from one, it is challenging to achieve ZVS for all switches and minimum circulating current [11], [12], [13], [14].

Voltage-fed resonant bidirectional dual active bridge (DAB) DC-DC converter :
A series resonant LC in DAB can eliminate the power transistor switching losses
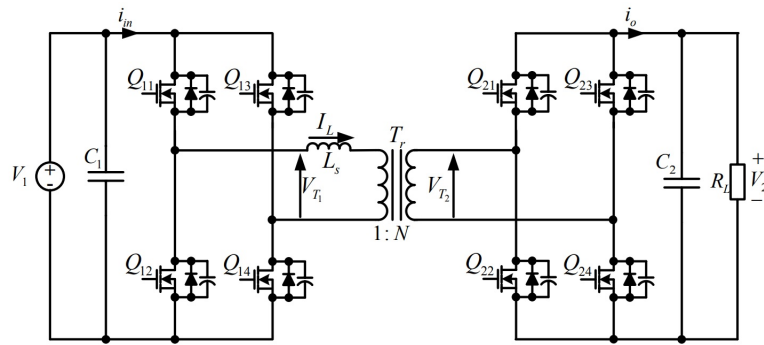
Figure 2.1: Voltage-fed isolated dual active bridge DC-DC converter [11].

in both full-bridge sides of the converter, full ZVS, and approximately ZCS are achieved in all the switches, see Figure 2.2. This allows for higher switching frequencies to be adopted and, consequently, it allows reducing the size of the magnetic components [15], [16], [17]. However, the resonant elements increase the complexity of the system and control method.

There are many types of DAB resonant converters proposed to improve the performance of the DAB such as DAB with CLC resonant circuit in [18], DAB with LLC in [19], DAB with CLLC in [20], etc.
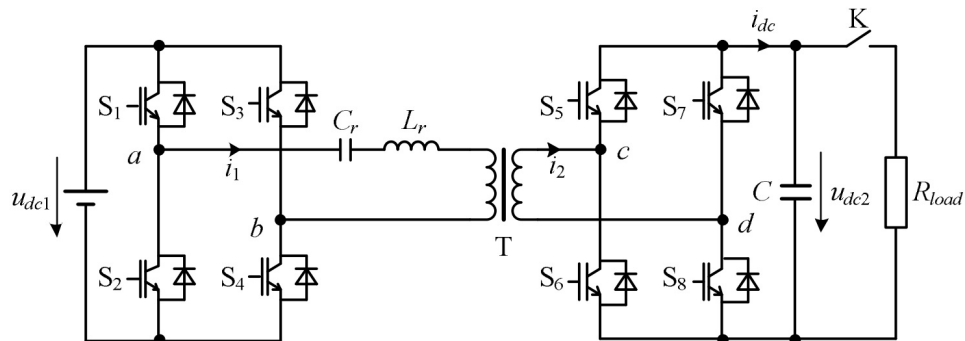
Figure 2.2: Voltage-fed isolated dual active bridge DC-DC converter with series resonant circuit [17].

Current-fed push-pull DC-DC converter:

The push-pull topology's advantages are a minimal number of switching devices, lower switching losses, isolation, and low input ripple current [21]. However, these advantages are achieved at the expense of a reduction in transformer utilization, higher conduction losses, and a higher switch voltage stress.

Therefore, to protect the switching devices an extra clamp snubber circuit is needed like all other types of current-fed topologies [22]. Figure 2.3 shows the push-pull CFC without a clamp circuit. Hence, to increase the power density, increase the transformer utilization, and reduces the stress on switches, a ZVS-

PWM current-fed push-pull converter is proposed in [23].
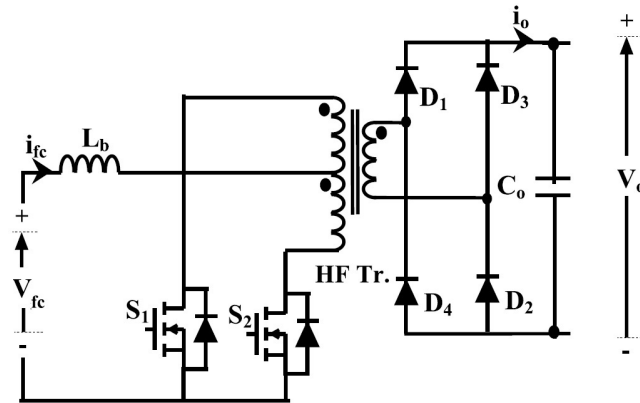
Figure 2.3: Current-fed isolated push-pull DC-DC converter.

Current-fed resonant DC-DC converter:
Some resonant versions of the current-fed converters with zero-current switching (ZCS) are proposed in [24], [25] to reduce the switching losses and the switches voltage stress of the CFC and thus improve the converter efficiency. The current-fed series resonant converter is shown in Figure 2.4.

The resonant CFC utilizes the leakage inductance, magnetizing inductance, and parasitic capacitance of the transformer to achieve ZCS and reduce the voltage spikes across the switches. An additional advantage of this configuration is that the rectifier diodes on the secondary side of the converter are operated with ZCS. Generally, the resonant converters increase the complexity of the converter design and required additional components. Furthermore, in general, they are generating a significant amount of circulating current in the full-bridge that adds to the conduction losses of the converter.
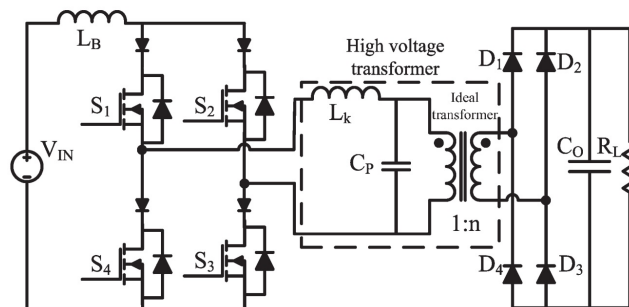
Figure 2.4: Current-fed isolated series resonant DC-DC converter.

Current-fed full-bridge and half-bridge DC-DC converter:
There are other two possible CFC topologies that can meet the FC requirements,

the half-bridge current-fed converter (L-type known as LTCFC) explained in [26] and the full-bridge current-fed converter (FBCFC) in [27]. Figure 2.5 shows the current-fed half-bridge DC-DC converter.

Both topologies have an energy storage inductor at the input, a high-frequency isolation transformer, and a diode rectifier bridge with smoothing filter capacitors at the output. Both configurations provide an inherent boost action, which results in a lower transformer ratio and a subsequent reduction in the leakage inductance, which improves the converter's performance. A half-bridge, compared to a full-bridge converter, has a smaller number of active devices but requires two DC inductors that carry a current ripple.

Both converters act as a controlled current source and are, therefore, suitable for an FC generator. The main disadvantages of these configurations are hard-switching operation and voltage spikes at turn-off across the elements due to the transformer leakage inductance that results in high conduction and switching losses. Consequently, the operating efficiency and the reliability of the converter will be reduced.
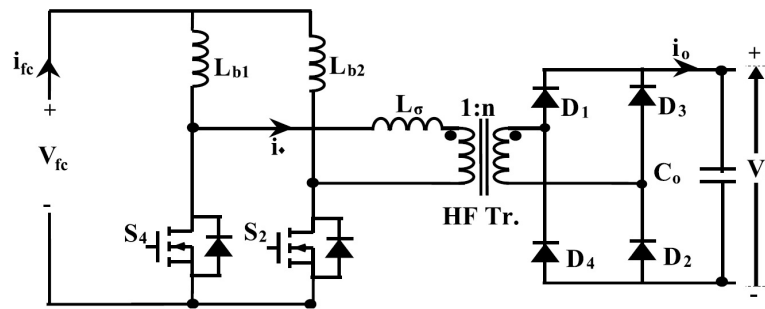
Figure 2.5: Current-fed isolated half-bridge DC-DC converter.

Current-fed full-bridge and half-bridge DC-DC converter with additional clamp circuit:

Passive or active clamps for LTCFC and FBCFC have been presented in [28], [29], [30]. The purpose of this extra circuit is to achieve ZVS and reduce or avoid the high voltage stress for the converter switches.

In a passive clamp circuit, the energy stored in the capacitance is dissipated on the snubber resistor; such a passive clamp circuit will reduce the converter efficiency. Active clamp circuits across the converter switches can be used to absorb the resonant leakage energy and recover it to the load whilst clamping the voltage across the switching devices. Figure 2.6a and Figure 2.6b show a current-fed isolated half-bridge converter with passive and active clamp circuit respectively.

This has the additional advantage of operating the main switches with ZVS at turn-on, thus improving converter efficiency and performance. Compared to the active clamp full-bridge CFC, the main drawbacks of the active clamp half-bridge CFC configuration are the use of more passive components and the

need for two active clamp circuits, thus increasing the complexity of the PWM
control circuit.
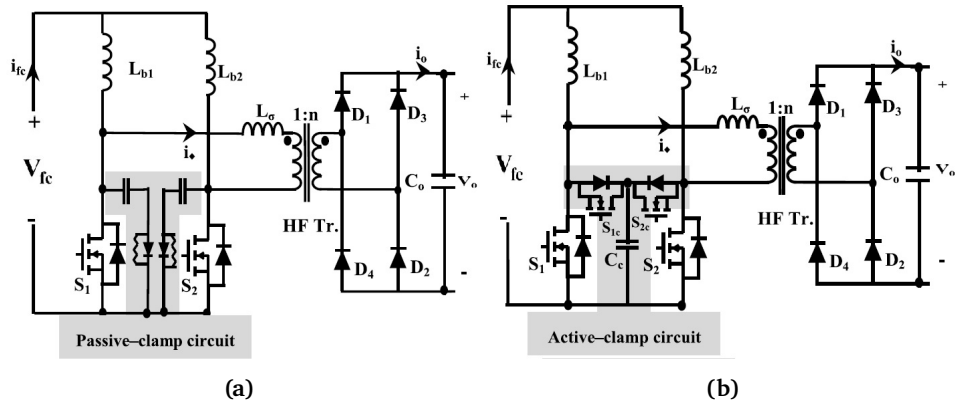
Figure 2.6: Current-fed isolated half-bridge DC-DC converter, (a) with passive clamp
circuit, (b) with active clamp circuit.

2.2 Operation and Analysis of the Current-Fed Full-Bridge Isolated DC-DC Converter With Active Clamp

As mentioned in Chapter 1, a current-fed full-bridge isolated DC-DC converter
with an active clamp circuit is selected to investigate in this thesis. Here, the
converter, shown in Figure 2.7, analysed and step by step its operation and
steady-states equations are driven and explained. [28]. Before going through
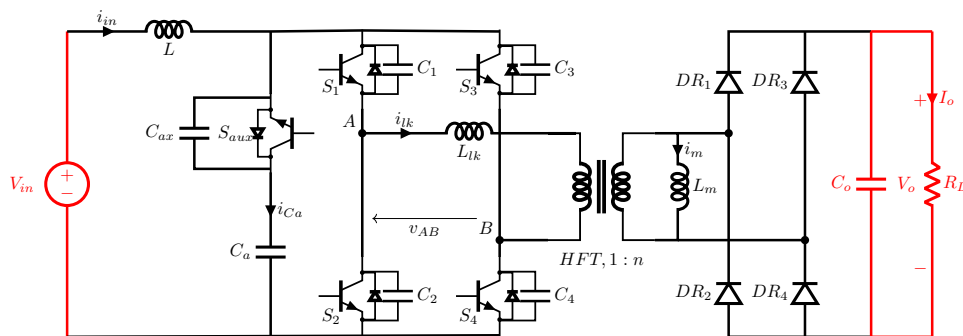
Figure 2.7: Current-fed full bridge DC-DC converter with active-clamp.

the calculation, the following assumptions were made for the operation and

analysis of the converter[31]:

1) Input boost inductor L is large enough so that the current through it, is considered constant.

2) Clamp capacitor C_a is large to keep the voltage across it constant.

3) All components including switches and diodes are ideal [32].

Switches S_1 and S_4 are operated by the common gating signals G_{S1}, and S_2 and S_3 are operated by gating signal of G_{S2}. Gating signals of these two legs of the converter are shifted by $180°$ with an overlap. The duty cycle of the main switches is always greater than 50% to prevent increased circulating current through the active clamp circuit [33]. This current circulation results in extra conduction losses which lowers converter performance, as the auxiliary circuit loss becomes comparable to the loss in the main switches.

The auxiliary switch S_{aux} in the clamp circuit, is controlled by a gating signal which is complementary to both main switches' gating signals (G_{Sax}) [7]. It means whenever one of the gate signals of G_{S1} or G_{S2} turns off, the auxiliary switch starts conducting. Then, the duty cycle of the auxiliary switch is always less than 50% and its switching frequency is double that of the main switches. The steady-state operating waveforms are shown in Figure 2.8 and the operation of the converter during different intervals is explained using the equivalent circuits.

Interval 1, ($t_0 < t < t_1$) : In this interval, all four main switches S_1 to S_4 are ON and auxiliary switch S_{aux} is OFF, see Figure 2.9. The input current flows through boost inductance. Power is transferred to the load by the energy stored in the output filter capacitor C_o. The only current circulating through the leakage inductance is transformer magnetizing current and given by

$$i_{lk} = i'_{Lm} = -I'_{Lm,peak}, \tag{2.1}$$

where i_{lk} is the leakage inductance current, i'_{Lm} is magnetizing current reflected to primary side and $I'_{Lm,peak}$ is the peak value of magnetizing current, given by

$$I'_{Lm,peak} = \frac{nV_o T_{DR}}{2L_m}. \tag{2.2}$$

Here n is secondary to primary transformer ratio and T_{DR} is rectifier diode conduction time.

Voltage across the auxiliary capacitor and switch are

$$V_{Ca} = V_{Sax} = \frac{V_{in}}{2(1 - D)}, \tag{2.3}$$

where the duty ratio of main switches $D = (T_{on}/T_s)$, T_{on} is conduction time of main switch and T_s is switching time period.

Interval 2, ($t_1 < t < t_2$) : As it is shown in Figure 2.10 at $t = t_1$, the main
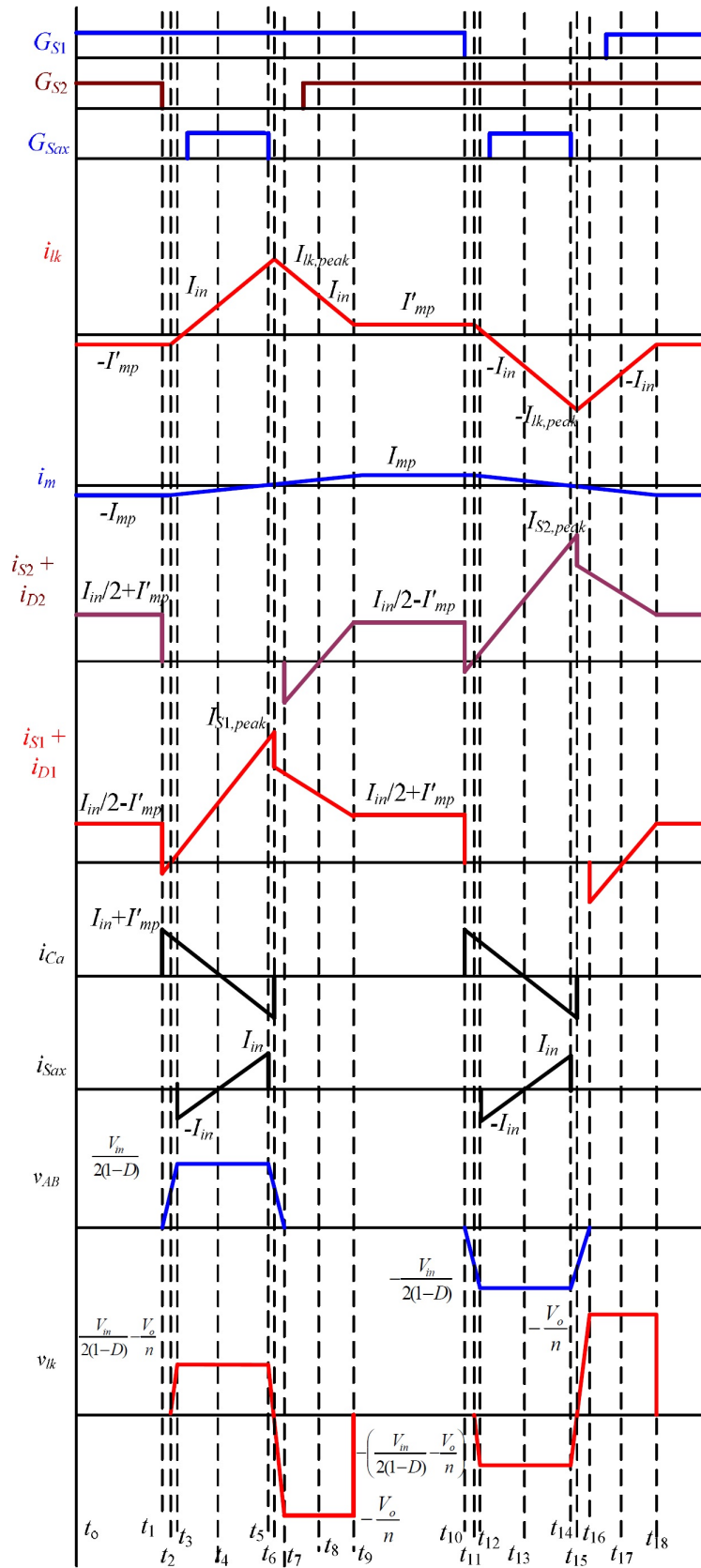
Figure 2.8: Steady-state operation waveforms of current-fed full bridge DC-DC converter with active-clamp[31].
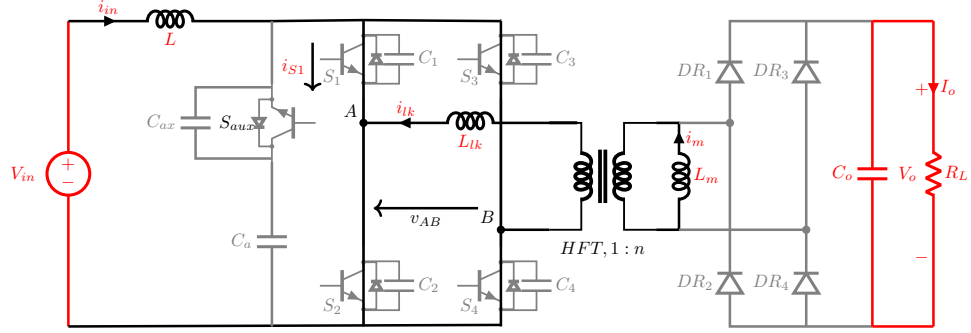
Figure 2.9: Operation of CFC, Interval 1.
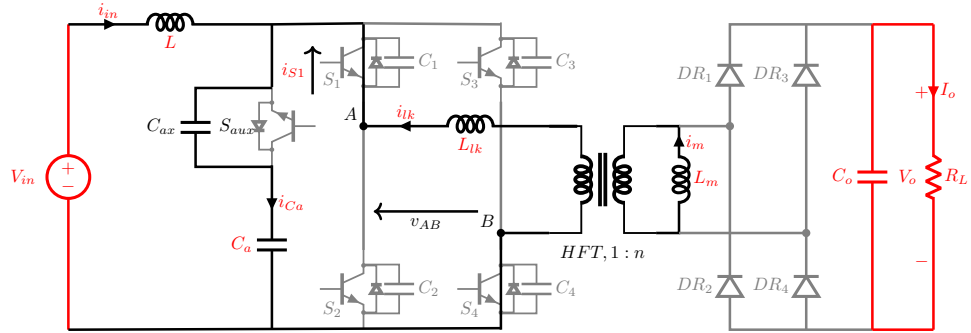
Figure 2.10: Operation of CFC, Interval 2.

switches S_2 and S_3 are turned OFF. Current in the input boost inductor is diverted into the clamp circuit path, the anti-parallel body diode D_{ax} of the auxiliary switch starts conducting and S_{aux} can be gated for ZVS turn on.

The magnetizing current flows through the leakage inductance, and the antiparallel diodes D_1 and D_4 of the main switches S_1 and S_4. Therefore, currents through S_1 and S_4 quickly drop to negative, which is the same value as the peak of reflected magnetizing current $I'_{Lm,peak}$. Capacitances C_2 and C_3 of the main switches S_2 and S_3 start charging and at the same time auxiliary capacitor C_{ax} starts discharging linearly. On the secondary side of converter, diodes are biased reversely, and power is still transferred to the load by the output capacitor.

The current ($I'_{Lm,peak}$) continues to flow through L'_m. At the end of this interval, voltages across the main switch S_2 and the auxiliary switch S_{aux} are

$$V_{S2}(t_2) = V_{S3}(t_2) = \frac{V_o}{n} \quad , \quad V_{Sax}(t_2) = V_{Ca} - \frac{V_o}{n}. \tag{2.4}$$

State equations for Interval 1 and 2 are given by

$$L\frac{di_L}{dt} = V_{in} \quad , \quad L_{lk}\frac{di_{lk}}{dt} = 0 \quad , \quad C_a\frac{dv_{Ca}}{dt} = 0 \quad , \quad C_o\frac{dv_o}{dt} = -\frac{v_o}{R_L}. \tag{2.5}$$

Interval 3, $(t_2 < t < t_3)$: Snubber capacitors which partially charged in interval
2, continue charging and discharging. The voltage across the main switches
v_{S2} and v_{S3} increases from V_o/n to V_{Ca}. The current through the leakage
inductance i_{lk} rises linearly and a voltage equal to $(V_{Ca} - V_o/n)$ appears across
it. The current through the magnetizing Inductance starts increasing linearly
and output voltage V_o falls across L_m. The rectifier diodes DR_1 and DR_4 are
forward biased as shown in Figure 2.11 and start conducting when the leakage
inductance current rises above i'_{Lm} and power is transferred to the load.
  The leakage inductance current and the current through the switch S_1 are
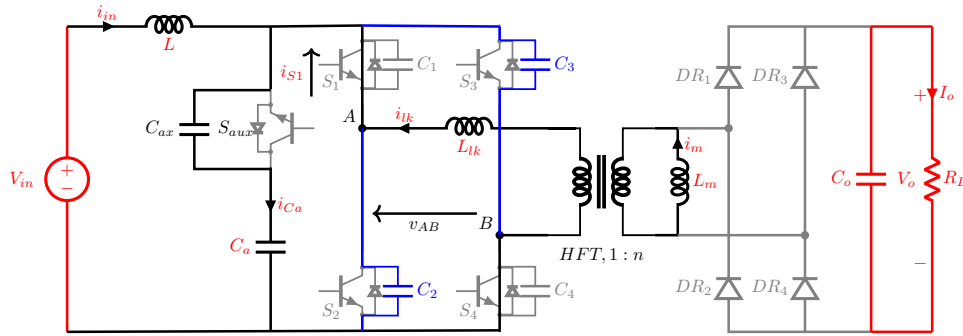
Figure 2.11: Operation of CFC, Interval 3.

equal and are given by

$$i_{lk} = i_{S1} = -I'_{Lm,peak} + \frac{v_{S2} - \left(\frac{V_o}{n}\right)}{L_{lk}}(t - t_2). \tag{2.6}$$

The magnetizing inductance current is

$$i_{Lm} = -I_{Lm,peak} + \frac{V_o}{L_m}(t - t_2), \tag{2.7}$$

where $I_{Lm,peak}$ is the the peak current through magnetizing inductance on
secondary side.
The auxiliary clamp capacitor current i_{Ca} falls linearly and the the current of
$I_{in} - i_{Ca}$ is transferred to the transformer through the switches S_1 and S_4 and
thus to the load.
At the end of this interval, the auxiliary capacitor is discharged completely to
zero and C_2 and C_3 are charged to their full voltage which are equal to V_{Ca}.
Final values are:

$$v_{Cax}(t_3) = v_{Sax}(t_3) = 0,$$

$$V_{Ca} = v_{S2}(t_3) = v_{S3}(t_3) = v_{C2}(t_3) = v_{C3}(t_3) = \frac{V_{in}}{2(1-D)}. \tag{2.8}$$

Interval 4, $(t_3 < t < t_4)$: In this interval, the body diode D_{ax} of the auxiliary
switch starts conducting and S_{aux} can be gated for ZVS turn on, shown in
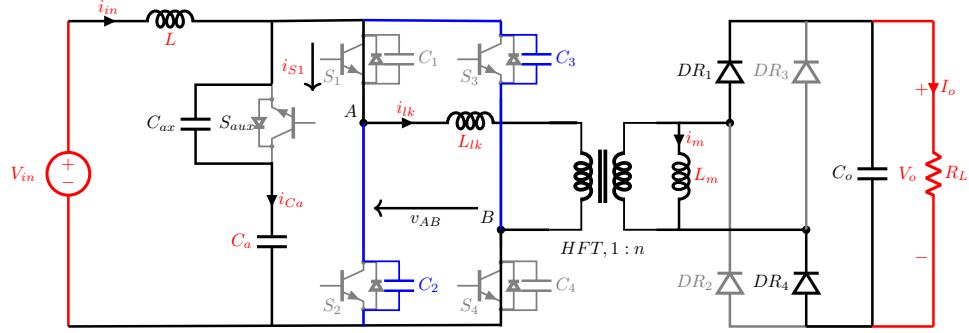
Figure 2.12: Operation of CFC, Interval 4.

Figure 2.12.

The current i_{lk} is increasing with the slope of $[(V_{Ca} - V_o/n)/L_{lk}]$. The current through S_1 and S_4 changes direction to positive magnitude. The transformer leakage inductance current and current throught S_1 are equal and given by

$$i_{lk} = i_{S1} = i_{lk}(t_3) + \frac{V_{Ca} - \left(\frac{V_o}{n}\right)}{L_{lk}}(t - t_3). \tag{2.9}$$

The current through the magnetizing inductance is increasing with the same slope as i_{lk} and is given by

$$i_{Lm} = i_{Lm}(t_3) + \frac{V_o}{L_m}(t - t_3). \tag{2.10}$$

The current through the clamp capacitor during this interval dropping and is given by

$$i_{Ca} = I_{Ca,peak} - \frac{V_{Ca} - \left(\frac{V_o}{n}\right)}{L_{lk}}(t - t_3). \tag{2.11}$$

The final values at the end of this interval are $i_{Ca}(t_4) = 0$, $i_{lk}(t_4) = i_{S1}(t_4) = i_{S4}(t_4) = I_{in}(t_4)$.

The state equations for interval 3 and 4 are

$$L\frac{di_L}{dt} = V_{in} - V_{Ca} \quad , \quad L_{lk}\frac{di_{lk}}{dt} = V_{Ca} - \frac{V_o}{n}$$
$$C_a\frac{dv_{Ca}}{dt} = i_L - i_{lk} \quad , \quad C_o\frac{dv_o}{dt} = \frac{i_{lk}}{n} - \frac{v_o}{R_L}. \tag{2.12}$$

Interval 5, $(t_4 < t < t_5)$: In this interval, the auxiliary switch is turned on with ZVS. The current i_{Ca} drops linearly below zero, and the current through leakage inductance increases above I_{in} with the same slope as interval 4, Figure 2.13. Besides, the magnetizing current is increasing with the same slope as interval 4. The equations for this interval are
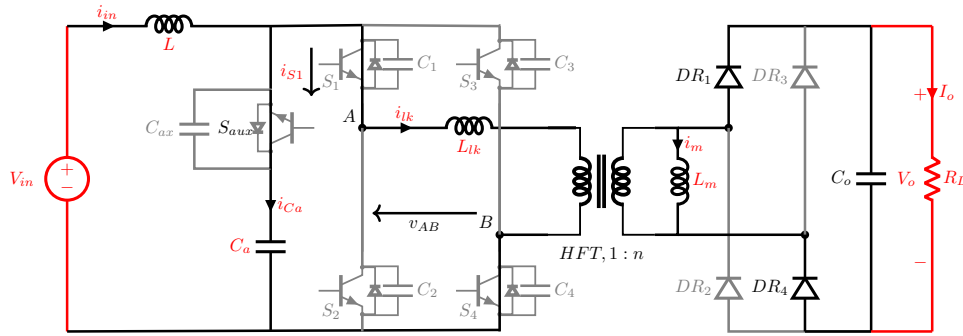
Figure 2.13: Operation of CFC, Interval 5.

$$i_{lk} = I_{in} + \frac{V_{Ca} - (\frac{V_o}{n})}{L_{lk}}(t - t_4), \tag{2.13}$$

$$i_{Ca} = I_{in} - i_{lk} = -\frac{V_{Ca} - (\frac{V_o}{n})}{L_{lk}}(t - t_4). \tag{2.14}$$

The switch current and its peak value are given by

$$i_{S1} = I_{in} + i_{Ca}$$
$$I_{S1,peak} = 2I_{in} + \frac{nV_o}{f_s L_m}(1 - D). \tag{2.15}$$

This interval ends when the current i_{Ca} reaches the negative peak of ($\bar{\ }(I_{in} + I'_{Lm,peak})$), and therefore the currents through the leakage inductance and the switch S_2 increase to their peak values. The final values are $i_{Ca}(t - 5) = -I_{Ca,peak}$, $i_{lk}(t_5) = I_{lk,peak}$, $i_{S1}(t_5) = I_{S1,peak}$.

Interval 6, ($t_5 < t < t_6$) : The auxiliary switch is turned off at $t = t_5$. C_{ax} is charegd and C_2 and C_3 are discharged by current i_{lk}, see Figure 2.14. The
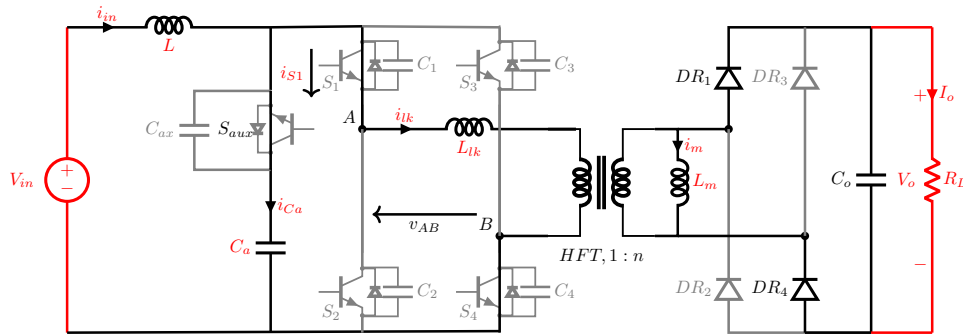
Figure 2.14: Operation of CFC, Interval 6.

leakage inductance resonates with the snubber capacitors C_{ax} and $C_2 + C_3$, and this value decreases by a small amount as this time interval is short. The

resonant frequency is given by

$$w_r = \frac{1}{\sqrt{L_{lk}(C_2 + C_3 + C_{ax})}}. \tag{2.16}$$

The voltages across the switch S_2 and the auxiliary switch S_{aux} are given by

$$v_{S2} = V_{Ca} - v_{Sax}, \tag{2.17}$$

$$v_{Sax} = I_{lk,peak}\sqrt{\frac{L_{lk}}{C_2 + C_3 + C_{ax}}}sin(w_r(t - t_5)). \tag{2.18}$$

Moreover, the current through the leakage inductance and the main switch are:

$$i_{lk} = I_{lk,peak}cos(w_r(t - t_5)) \tag{2.19}$$

$$i_{S1} = I_{S1,peak}cos(w_r(t - t_5)) \tag{2.20}$$

At the end of this interval, C_2 and C_3 discharge to V_o/n and C_{ax} charges to$(V_{Ca} - V_o/n)$. The final values are (neglecting small increase in current in this short interval)

$$v_{Sax}(t_6) = V_{Ca} - \frac{V_o}{n} \quad , \quad v_{S2}(t_6) = \frac{V_o}{n}. \tag{2.21}$$

The current i_{in} increases with the same slope as interval 3,4 and the state equations as that of interval 3,4 hold true for interval 5,6 too.

Interval 7, $(t_6 < t < t_7)$: The current i_{lk} is still charging C_{ax} to its final value and discharging C_2, C_3 completely to zero. It is a short interval as well, and the current through the leakage inductance decreases very little in this interval, Figure 2.15. The final values at the end of this interval are $v_{S2}(t_7) = 0$, $v_{Sax}(t_7) = V_{Ca}$.

Interval 8, $(t_7 < t < t_8)$: In this interval, the antiparallel body diodes of the main switch S_2 and S_3 start conducting and these switches can be gated for ZVS turn on, Figure 2.16. The current i_{lk} drops with a negative slope and it can be calculated by

$$i_{lk} = I_{lk}(t_7) - \frac{V_o}{nL_{lk}}(t - t_7), \tag{2.22}$$

$$i_{D2} = i_{lk} - I_{in}. \tag{2.23}$$

This interval ends when current $i_{lk} = I_{in}$. The final values are $i_{D2}(t_8) = 0$, $i_{lk}(t_8) = I_{in}$. The state equation for interval 7 and 8 are given by

$$L\frac{di_L}{dt} = V_{in} \quad , \quad L_{lk}\frac{di_{lk}}{dt} = -\frac{V_o}{n},$$
$$C_a\frac{dv_{Ca}}{dt} = 0 \quad , \quad C_o\frac{dv_o}{dt} = \frac{i_{lk}}{n} - \frac{v_o}{R_L}. \tag{2.24}$$
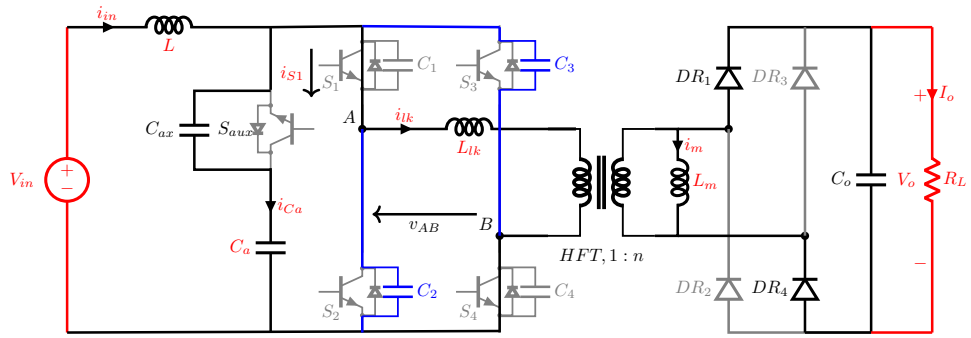
Figure 2.15: Operation of CFC, Interval 7.
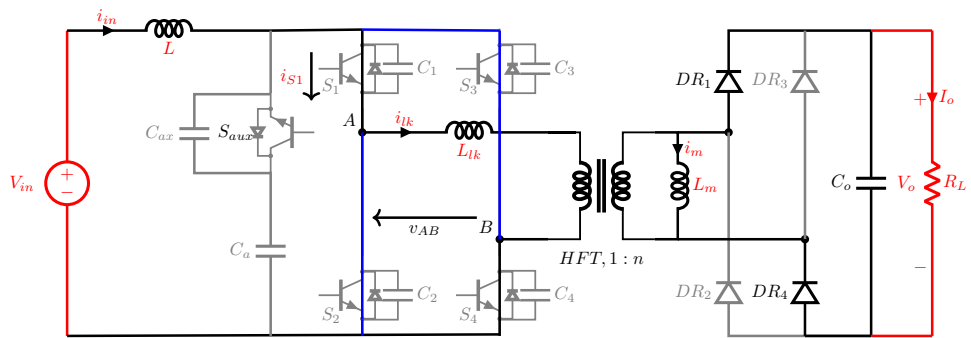
Figure 2.16: Operation of CFC, Interval 8.

Interval 9, ($t_8 < t < t_9$) : In this interval, switches S_2 and S_3 are turned on with ZVS. As it is shown in Figure 2.17, the currents i_{S2} and i_{S3} start increasing, and the current i_{lk} is transferred to the switches S_2 and S_3 and dropps with the same slope. The interval ends when the current i_{lk} equals the current i'_{Lm}. Currents i_{S2} and i_{S3} reache $[I_{in}/2 - I'_{Lm,peak}]$, and i_{S1} and i_{S4} reache to $[I_{in}/2 + I'_{Lm,peak}]$. Same state equations as that of interval 7,8 hold true for this interval too.
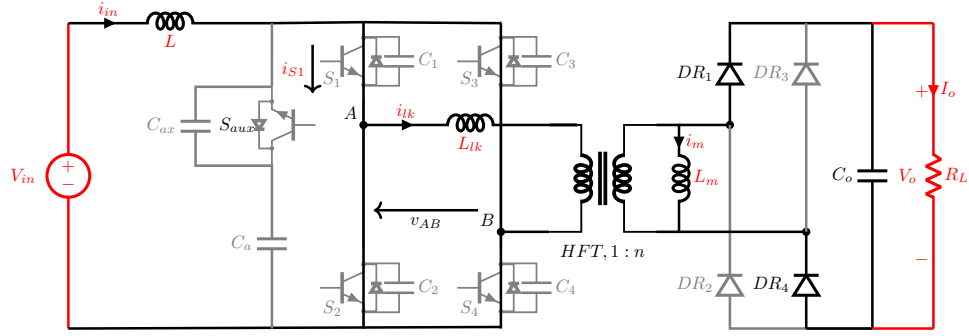
Figure 2.17: Operation of CFC, Interval 9.

$$i_{lk} = I_{in} - \frac{V_o}{nL_{lk}}(t - t_8), \tag{2.25}$$

$$i_{S2} = \frac{V_o}{nL_{lk}}(t - t_8), \tag{2.26}$$

$$i_{S1} = I_{in} + \frac{V_o}{nL_{lk}}(t - t_8), \tag{2.27}$$

At the end of the interval, the values are $i_{S2}(t_9) = I_{in}/2 - I'_{Lm,peak}$, $i_{S1}(t_9) = I_{in}/2 + I'_{Lm,peak}$, $i_{lk}(t_9) = i'_{Lm}(t_9) = I'_{Lm,peak}$.

For the next half-cycle, the intervals are repeated in the same sequence to complete the full cycle. The design equations for the converter are derived based on the above analysis and presented in the next section.

2.3 Converter Design

In this chapter, the converter design procedure is illustrated with a converter of variable input voltage $V_{in,min} = 800V$ to $V_{in,max} = 1000V$, fixed output voltage (DC voltage link) $V_o = 1000V$, output power $P_o = 400kW$, and switching frequency $f_s = 20kHz$.

Input current ($I_{in,av}$): The system is assumed to be ideal and (η) is 100%,

the average input current is given by

$$I_{in,av} = \frac{P_{in}}{V_{in}} = \frac{P_o}{\eta V_{in}}. \tag{2.28}$$

The average input current at the minimum voltage in the curcuit is: $I_{in,av} = 500A$.

Duty cycle of main switches(D_{max}): D_{max} is selected at the minimum input voltage and have a reverse relation with the maximum switch voltage rating

$$V_{sw,max} = \frac{V_{in,min}}{2(1 - D_{max})}, \tag{2.29}$$

where for $D_{max} = 80\%$, the maximum switch voltage rating is $V_{sw,max} = 2kV$.

Leakage Inductance (L_{lk}) and magnetizing inductance (L_m): The inductance values for a chosen rated power P_o and switching frequency f_s depends upon the transformer turns ratio n, inductor ratio L'_m/L_{lk} and the maximum duty cycle D_{max} calculated earlier. Where L'_m is equivalent magnetizing inductance referred to primary side of transformer. The leakage inductance is obtained from current waves through leakage inductance i_{lk} and magnetizing inductance i_{Lm}

$$L_{lk} = \frac{R_L}{f_s} \left[\frac{(\frac{V_{in}}{V_o})^2}{4(1 + \frac{L_{lk}}{L'_m})} - \frac{(\frac{V_{in}}{V_o})(1 - D_{max})}{2n} \right], \tag{2.30}$$

where n, the secondary to primary transfer ratio, is selected to maintain duty cycle of the main switches is bigger that 0.5. R_L is the load and considered to be $R_L = V_o/P_o$. D is given by rewriting the above equation

$$D = 1 - \frac{2nV_o}{V_{in}} \left[\frac{(\frac{V_{in}}{V_o})^2}{4(1 + \frac{L_{lk}}{L'_m})} - \frac{L_{lk}f_s}{R_L} \right]. \tag{2.31}$$

Also, n must be such that L_{lk} is positive in below eq. (2.32).

$$n > 2(1 - D_{max})(1 + \frac{L_{lk}}{L'_m})\frac{V_o}{V_{in}} \tag{2.32}$$

The above equation shows if the value of magnetizing inductance is considered very large $L_m = \infty$, the minimum value of turn ratio is 0.5.

Moreover, the inductance ratio L'_m/L_{lk} is selected based on the ZVS range, and main switch RMS current which is given by

$$I_{sw,rms} = \sqrt{I_{in,av}^2 \left[0.75 - \frac{D}{2} + \frac{f_s T_{DR}}{3} \right] + (I'_{Lm,peak})^2 \left[\frac{2}{3} + \frac{D}{3} - \frac{4f_s T_{DR}}{3} \right] + I_{in,av} I'_{Lm,peak} \left[D - 1 + \frac{f_s T_{DR}}{3} \right]}. \tag{2.33}$$

Where T_{DR} is the rectifier diode conduction time after neglecting short duration of the snubber charging/discharging, given by

$$T_{DR} = \frac{nV_{in}}{2V_o f_s \left(1 + \frac{L_{lk}}{L'_m} \right)}. \tag{2.34}$$

Figure 2.18 shows variation of the leakage inductance $[H]$, and the switch RMS current $[A]$, with respect to the inductance ratio L'_m/L_{lk} for five values of the transformer turns ratio n. It can be seen that smaller value of L'_m/L_{lk} will achieve ZVS but increases the currents through the switches, reducing the efficiency of the converter [33].

For the higher transformer turns ratio, $n = 5$, value of L_{lk} is high and increases
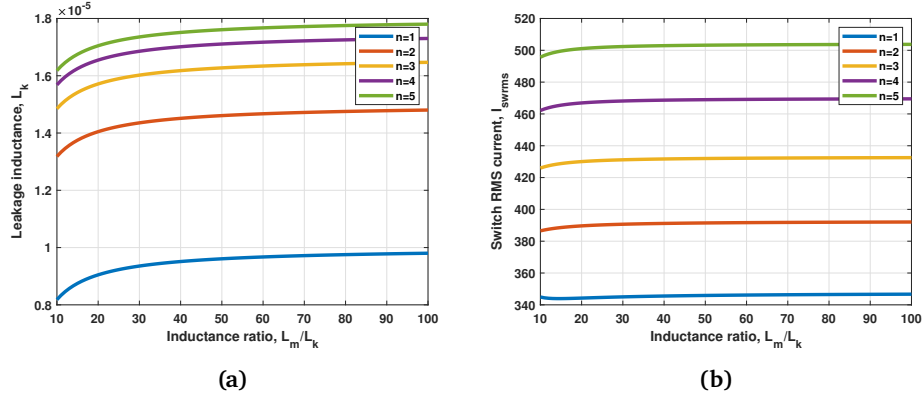
Figure 2.18: (a)Leakage inductance value vs inductance ratio and turn ratio of transformer, (b)Switch RMS current vs inductance ratio and turn ratio of transformer.

ZVS range. Furthermore, for the turn ratio $n > 2$, the duty cucle of main switches are less than 0.5, and as the auxiliary switch duty cycle is $D_{Sax} = 2(1 - D)$, selecting the duty cycle of main switches D lower than 0.5 results in $D_{Sax} >= 1$, which is impossible.

Choosing a design with a smaller value of D, say 0.6 for example (instead of 0.8), will result in a smaller value of L_{lk}, which might not be able to store sufficient energy to maintain ZVS. Based on the above discussion, transformer ration $n = 1$ is selected. As **??** shows, reduction in the RMS current is negligible for $L'_m/L_{lk} > 20$ and the selected value of n.

Therefore, an inductance ratio of $L'_m/L_{lk} = 20$ is choosen. Using $D_{max} = 0.8$, $n = 1$, and $L'_m/L_{lk} = 20$, calculated values of the inductances are $L_{lk} = 9.04\mu H$ and $L_m = 0.18mH$.

Input boost inductance (L): The value of input inductor is given by

$$L = \frac{V_{in}(D - 0.5)}{\Delta I_{in} f_s}, \tag{2.35}$$

where ΔI_{in} is the boost inductor ripple current. For the value of $\Delta I_{in} = 0.5A$, $L = 8mH$.

Inductors' rating: The peak current through the magnetizing inductance is calculated to be $I'_{Lm,peak} = I_{Lm,peak} = 52.63A$ by eq. (2.2). The peak current through the leakage inductance is $I_{lk,peak} = 2I_{in} + I'_{Lm,peak} = 1052.63A$. The

maximum voltage across L_{lk} is $V_o/n = 1000V$ and across L_m is $V_o = 1000V$.

Main switchs' rating: The peak and average currents through the main switches are $I_{sw,peak} = 2I_{in} + I'_{Lm,peak} = 1052.63A$ and $I_{sw,av} = I_{in}/2 = 250A$, respectively. The RMS value of main switches' currents is $371.56A$ which can be calculated by eq. (2.33).

Auxiliary switch's rating: The peak current through the auxiliary switch is $I_{aux,peak} = I_{in} + I'_{Lm,peak} = 552.63A$ and the average current through it, is $55.26A$ given by

$$I_{aux,av} = (I_{in} + I'_{Lm,peak})\left[\frac{(1-D)}{4}\right]. \tag{2.36}$$

Moreover, the RMS current through the auxiliary switch is $285.38A$ calculated by

$$I_{aux,rms} = (I_{in} + I'_{Lm,peak})\sqrt{\frac{2(1-D)}{3}}. \tag{2.37}$$

Auxiliary clamp capacitor (C_a): The peak and RMS current through C_a are the same as the auxiliary switch, $I_{Ca,peak} = 552.63A$ and $I_{Ca,rms} = 285.38A$, respectively. The value of the auxiliary capacitor is

$$C_a = \frac{(1-D)^2}{\pi^2 f_s^2 L_{lk}}. \tag{2.38}$$

The value of the clamp capacitor is $C_a = 4.56\mu F$.

Snubber capacitor (C_{ax}): The snubber capacitor is given by

$$C_1 + C_4 + C_{ax} = \frac{t_f(I_{in} + I'_{Lm,peak})}{V_{in}/2(1-D)}, \tag{2.39}$$

where t_f is all time of the switches during turn-off. The calculated value of the snubber capacitor across the auxiliary switch is $C_{ax} = 0.356nF$. The snubber capacitor's voltage rating is equal to the switch voltage, given by eq. (2.3) and is $2000V$.

Output capacitor (C_o): The value of the output filter capacitor is

$$C_o = \frac{I_o\left(\frac{1}{2f_s} - T_{DR}\right)}{\Delta V_o}, \tag{2.40}$$

where ΔV_o is the ripple output voltage. With $\Delta V_o = 0.75V$, the output capacitor is $C_o = 3.2mF$. The designed values are summarized in the Table 2.1

2.4 Small-Signal Analysis

Steady-state operating waveforms, the state-space equation, and the equivalent circuits of the converter for each interval are discussed in section 2.2. In this

Table 2.1: Values of the Parameters Obtained from Designed Equations

Specifications	Symbol	values	Specifications	Symbol	values
Input voltage	V_{in}	$800 - 1000V$	Input inductor	L	$8mH$
Output voltage	V_o	$1000V$	Leakage inductor	L_{lk}	$9.04\mu H$
Output power	P_o	$400kW$	Magnetizing inductor	L_m	$0.18mH$
Switching frequency	f_s	$20kHz$	Output capacitor	C_o	$3.2mF$
Transformer turn ratio	n	1	Auxiliary Capacitance	C_a	$4.56\mu F$

section, the small-signal AC model is derived based on state-space averaging. For the analysis, assumptions made are:

1. Charging and discharging intervals of snubber capacitors are very small and neglected.

2. The leakage inductance of the transformer is part of L_{lk}.

3. The magnetizing inductance is assumed to be very large ($i_{Lm} = 0$) and neglected.

4. All the components are ideal and lossless [34].

The state equations are averaged over a full cycle. Since i_L is discontinuous, the average value for the rate of change of leakage current over one complete cycle is zero $L_{lk}\langle\frac{di_{lk}}{dt}\rangle = 0$ then the state variable i_L can be omitted for the rest of Analysis. Averaging the state equations of other state variables over a complete cycle gives

$$L\left\langle\frac{di_{in}}{dt}\right\rangle = v_{in} - 2(1-d)v_{Ca}, \tag{2.41}$$

$$C_a\left\langle\frac{dv_{Ca}}{dt}\right\rangle = 2[i_{in}(1-d) - i_{lk}(1-d)], \tag{2.42}$$

$$C_o\left\langle\frac{dv_o}{dt}\right\rangle = i_{lk,rect,av} - \frac{v_o}{R_L}, \tag{2.43}$$

where $i_{lk,rect,av}$ is the average rectified current of the leakage indutance and given by

$$i_{lk,rect,av} = \frac{2i_{in}}{n}(d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9). \tag{2.44}$$

Where $d_3 = t_3 - t_2$ and so on.

Applying volt-sec balance across the series inductor during positive half cycle gives

$$\left(v_{Ca} - \frac{v_o}{n}\right)(d_3 + d_4 + d_5 + d_6) = \frac{v_o}{n}(d_7 + d_8 + d_9). \tag{2.45}$$

Simplifying the equations in terms of the duty cycles results in the following equations

$$C_a\left\langle\frac{dv_{Ca}}{dt}\right\rangle = 2i_{in}(1-d) - \frac{1}{f_s L_{lk}}\left(v_{Ca} - \frac{v_o}{n}\right)(1-d)^2, \tag{2.46}$$

$$C_o \left\langle \frac{dv_o}{dt} \right\rangle = \frac{2i_{in}}{n}(1 - d + d'') - \frac{v_o}{R_L}, \tag{2.47}$$

$$\left(v_{Ca} - \frac{v_o}{n}\right)(1 - d) = \frac{v_o}{n}d'', \tag{2.48}$$

Where d is duty cycle of the main switches $d = d_1 + d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10} + d_{17} + d_{18}$. Turn off period of the main switches is $(1 - d) = d_2 + d_3 + d_4 + d_5 + d_6 + d_7 = d_{11} + d_{12} + d_{13} + d_{14} + d_{15} + d_{16}$. And, conduction time of the auxiliary switch is $d'' = d_4 + d_5 = d_{13} + d_{14}$. Introducing perturbation around the steady state value for the state variables and other quantities such that $i_{in} = I_{in} + \hat{i}_{in}$, $v_{Ca} = V_{Ca} + \hat{v}_{Ca}$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$, $d = D + \hat{d}$ (D is the duty cycle of the main switches) and the same way for other intervals. With neglecting the second order terms, the steady-state equations eq. (2.41), eq. (2.46)-eq. (2.48) can be rewritten as the following equations

$$L\frac{d\hat{i}_{in}}{dt} = \hat{v}_{in} - 2\hat{v}_{Ca}(1 - D) + 2V_{Ca}\hat{d}. \tag{2.49}$$

$$C_a\frac{d\hat{v}_{Ca}}{dt} = 2\hat{i}_{in}(1 - D) - 2I_{in}\hat{d} - \frac{1}{f_s L_{lk}}\left(\hat{v}_{Ca} - \frac{\hat{v}_o}{n}\right)(1 - D)^2 + \frac{2}{f_s L_{lk}}\left(V_{Ca} - \frac{V_o}{n}\right)(1 - D)\hat{d}. \tag{2.50}$$

$$C_o\frac{d\hat{v}_o}{dt} = \frac{2\hat{i}_{in}}{n}(1 - D + D'') - \frac{2I_{in}}{n}(\hat{d} - \hat{d}'') - \frac{\hat{v}_o}{R_L}. \tag{2.51}$$

$$\left(\hat{v}_{Ca} - \frac{\hat{v}_o}{n}\right)(1 - D) - \left(V_{Ca} - \frac{V_o}{n}\right)\hat{d} = \frac{\hat{v}_o}{n}D'' + \frac{V_o}{n}\hat{d}''. \tag{2.52}$$

Taking Laplace transform of eq. (2.49)-eq. (2.52) results in following equations

$$sL\hat{i}_{in}(s) = \hat{v}_{in}(s) - 2\hat{v}_{Ca}(s)(1 - D) + 2V_{Ca}\hat{d}(s), \tag{2.53}$$

$$sC_a\hat{v}_{Ca}(s) = 2\hat{i}_{in}(s)(1 - D) - 2I_{in}\hat{d}(s) - \frac{1}{f_s L_{lk}}\left(\hat{v}_{Ca}(s) - \frac{\hat{v}_o(s)}{n}\right)(1 - D)^2 + \\ \frac{2}{f_s L_{lk}}\left(V_{Ca} - \frac{V_o}{n}\right)(1 - D)\hat{d}(s), \tag{2.54}$$

$$sC_o\hat{v}_o(s) = \frac{2\hat{i}_{in}(s)}{n}(1 - D + D'') - \frac{2I_{in}}{n}(\hat{d}(s) - \hat{d}''(s)) - \frac{\hat{v}_o(s)}{R_L}, \tag{2.55}$$

$$\left(\hat{v}_{Ca}(s) - \frac{\hat{v}_o(s)}{n}\right)(1 - D) - \left(V_{Ca} - \frac{V_o}{n}\right)\hat{d}(s) = \frac{\hat{v}_o(s)}{n}D'' + \frac{V_o}{n}\hat{d}''(s). \tag{2.56}$$

Eliminating $\hat{d}''(s)$ using eq. (2.56) and solving eq. (2.55) gives

$$\left(sC_o + \frac{1}{R_L}\right)\hat{v}_o(s) = \frac{2\hat{i}_{in}(s)}{n}(1 - D + D'' - \frac{2I_{in}}{n}\hat{d}(s) - \frac{2I_{in}}{V_o}\left(V_{Ca} - \frac{V_o}{n}\right)\hat{d}(s) + \\ \frac{2I_{in}}{V_o}(1 - D)\hat{v}_{Ca}(s) - \frac{2I_{in}}{nV_o}(1 - D + D'')\hat{v}_o(s). \tag{2.57}$$

Rearrenging eq. (2.57) and writing the steady-state variables in matrix form, results in

$$\begin{bmatrix} \hat{i}_{in}(s) \\ \hat{v}_{Ca}(s) \\ \hat{v}_o(s) \end{bmatrix} = [M(s)].\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix}.\hat{d}(s) + [M(s)].\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}.\hat{v}_{in}(s). \qquad (2.58)$$

Above equation presents the small signal model of the converter in matrix form where

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 2V_{Ca} \\ 2\left[\frac{1-D}{f_s L_{lk}}\left(V_{Ca} - \frac{V_o}{n}\right) - I_{in}\right] \\ -\frac{2I_{in}V_{Ca}}{V_o} \end{bmatrix} \qquad (2.59)$$

and

$$[M(s)] = \begin{bmatrix} sL & 2(1-D) & 0 \\ -2(1-D) & sC_a + \frac{(1-D)^2}{f_s L_{in}} & -\frac{(1-D)^2}{n f_s L_{in}} \\ -\frac{2(1-D+D'')}{n} & -\frac{2I_{in}(1-D)}{V_o} & sC_o + \frac{1}{R_L} + \frac{2I_{in}(1-D+D'')}{nV_o} \end{bmatrix}^{-1} \qquad (2.60)$$

The inverse matrix $(M(s))$ is presented as follow

$$[M(s)] = \begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ M_{31} & M_{32} & M_{33} \end{bmatrix} \qquad (2.61)$$

Where

$$M_{11} = (C_o C_a)s^2 + \left[\frac{(1-D)^2 C_o}{f_s L_{lk}} + C_a\left[\frac{1}{R_L}, +\frac{2I_{in}(1-D+D'')}{nV_o}\right]\right],$$

$$M_{12} = -[2(1-D)C_o]s - 2(1-D)\left[\frac{1}{R_L} + \frac{2I_{in}(1-D+D'')}{nV_o}\right],$$

$$M_{13} = -\frac{2(1-D)^3}{n f_s L_{lk}},$$

$$M_{21} = [2(1-D)C_o]s + 2(1-D)\left[\frac{1}{R_L} + \frac{2I_{in}(1-D+D'')}{nV_o}\right] + \frac{2(1-D)^2(1-D-D'')}{n^2.f_s L_{in}},$$

$$M_{22} = (LC_o)s^2 + L\left[\frac{1}{R_L} + \frac{2I_{in}(1-D+D'')}{nV_o}\right]s,$$

$$M_{23} = \frac{L(1-D)^2}{n f_s L_{lk}}s,$$

$$M_{31} = \frac{2C_a(1-D-D'')}{n}s + \frac{2(1-D)^2(1-D+D'')}{n f_s L_{lk}} + \frac{4I_{in}(1-D)^2}{V_o},$$

$$M_{32} = \frac{2I_{in}L(1-D)}{V_o}s - \frac{4(1-D)(1-D+D'')}{n},$$

$$M_{33} = (LC_a)s^2 + \frac{L(1-D)^2}{f_s L_{lk}}s + 4(1-D)^2.$$

$$(2.62)$$

The transfer functions can be calculated from this model and can be used for the closed-loop control system design of the converter.

2.5 Controller Design

The output of the converter is controlled by the various duty cycle of the main switches, which means the duty cycle is an input to the total transfer function while the converter output voltage is the output of it. Control to output transfer function can be obtained from eq. (2.58) by setting $\hat{v}_{in} = 0$. It results in the following equation

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{1}{|M(s)|} \begin{bmatrix} M_{31} & M_{32} & M_{33} \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3. \end{bmatrix} \tag{2.63}$$

The converter specifications and the designed values of the components are listed in Table 2.1. The control to the output voltage transfer function (TF) is calculated in MATLAB given by

$$TF = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-1.358e06s^2 + 1.289e11s + 2.603e12}{s^3 + 6.242e04s^2 + 1.917e07s + 6.683e08}. \tag{2.64}$$

The bode plot of the control to output voltage transfer function given by eq. (2.64) is shown in Figure 2.19. The phase margin (PM) and the gain margin (GM) of the uncompensated system is negative which means the system is unstable for small disturbances. The two-loop average current control based closed-loop controller is designed for compensating the system.

The control system block diagram, shown in Figure 2.20, consists of an inner current control loop and an outer voltage control loop. The voltage control loop provides the reference signal for the input inductor current. Fuel cells are very sensitive to input current ripples. The key to ripple reduction is to control the average boost inductor current to be DC, which requires that bandwidths of voltage and current loops are separated far apart with a slow voltage loop and a fast current loop [35].

2.5.1 Design of Current Control Loop

The objective of this section is to design PI controller parameters in order to achieve certain stability and responce criteria. The input boost inductor current to the duty cycle transfer function of the current loop is obtained given
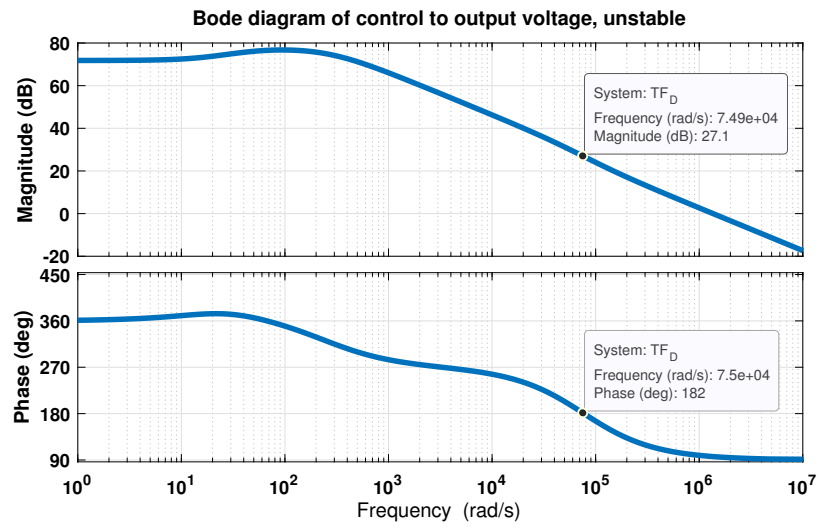
Figure 2.19: Bode diagram of control to output voltage TF without controller.
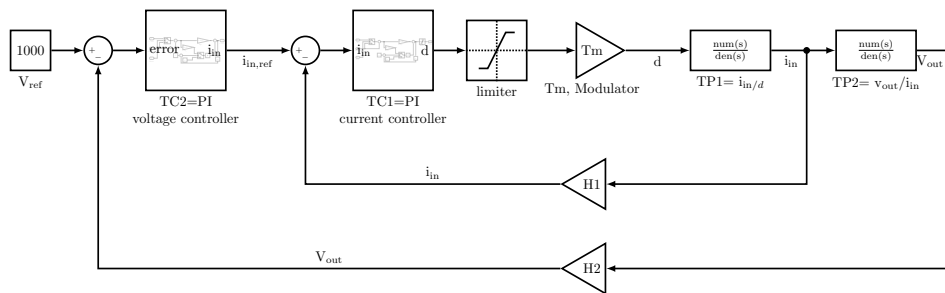
Figure 2.20: Two loop controll block system (voltage and current controller).

by

$$T_{p1} = \frac{\hat{i}_{in}(s)}{\hat{d}(s)} = \frac{1}{|M(s)|} \begin{bmatrix} M_{11} & M_{12} & M_{13} \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} \qquad (2.65)$$

which results in the below transfer function for the current controller loop

$$T_{p1} = \frac{1.666e05s^2 + 1.838e10s + 6.513e12}{s^3 + 6.242e04s^2 + 1.917e07s + 6.683e08}. \qquad (2.66)$$

The output of the current controller is converted from analog to digital and used as a duty cycle to control the main switches. The open loop transfer function of the current controller loop given by

$$G_{OL,c} = T_{c1}.T_m.T_{p1}.H_1, \qquad (2.67)$$

where T_{c1} is the current PI controller transfer function. Considering the gain of ADC and succeeding digital process, the gain of the modulator is $T_m = 1$. Also, the current feedback gain is assumed to be $H_1 = 1$. For simplicity of the calculations, T_{p1} and T_{c1} are consider as below

$$T_{p1}(s) = \frac{as^2 + bs + c}{ds^3 + es^2 + fs + g}, \qquad (2.68)$$

$$T_{c1}(s) = k_{p,c} + \frac{k_{i,c}}{s} = \frac{k_{p,c}s + k_{i,c}}{s}. \qquad (2.69)$$

The open loop transfer function can be written

$$\begin{aligned} G_{OL,c}(s) &= \left(\frac{as^2 + bs + c}{ds^3 + es^2 + fs + g}\right).\left(\frac{k_{p,c}s + k_{i,c}}{s}\right) \\ &= \frac{ak_{p,c}s^3 + ak_{i,c}s^2 + bk_{p,c}s^2 + bk_{i,c}s + ck_{p,c}s + ck_{i,c}}{ds^4 + es^3 + fs^2 + gs}. \end{aligned} \qquad (2.70)$$

By replacing jw_c instead of s in the above equation, and rearrenging

$$G_{OL,c}(jw_c) = \frac{\left(-ak_{i,c}w_c^2 - bk_{p,c}w_c^2 + ck_{i,c}\right) + j\left(-ak_{p,c}w_c^3 + bk_{i,c}w_c + ck_{p,c}w_c\right)}{\left(dw_c^4 - fw_c^2\right) + j\left(-ew_c^3 + gw_c\right)}. \qquad (2.71)$$

In order to have a stable system with overshoot of less than 10%, the amplitude of the open loop transfer function must be 1, and the phase margin is set to be 60 degrees at defined cross over frequency (w_c), which means

$$\begin{aligned} \left|G_{OL,c}\right|_{s=jw_c} &= 1, \\ \angle G_{OL,c}\Big|_{s=jw_c} &= -\pi + 60° = -120°. \end{aligned} \qquad (2.72)$$

The cross-over frequency is selected one order lower than the switching frequency, ($w_c = 2.\pi.2000 = 12560 rad/s$). Simplified equation of the magnitude of $G_{OL,c}$ in $s = jw_c$ is

$$\left| G_{OL,c} \right|_{s=jw_c} = \frac{\sqrt{\left(-ak_{i,c}w_c^2 - bk_{p,c}w_c^2 + ck_{i,c} \right)^2 + \left(-ak_{p,c}w_c^3 + bk_{i,c}w_c + ck_{p,c}w_c \right)^2}}{\sqrt{\left(dw_c^4 - fw_c^2 \right)^2 + \left(-ew_c^3 + gw_c \right)^2}}.$$

(2.73)

Replacing known parameters in eq. (2.73) and considering the above condition results in

$$\left| G_{OL,c} \right|_{s=12560j} = \sqrt{3.4037e - 6k_{i,c}^2 + 536.9479k_{p,c}^2}$$

$$= 1.$$

(2.74)

Appling the second condition for the angle of open loop transfer function, the second equation is reached

$$\angle G_{OL,c} \Big|_{s=jw_c} = \arctan\left(\frac{-ak_{p,c}w_c^3 + bk_{i,c}w_c + ck_{p,c}w_c}{-ak_{i,c}w_c^2 - bk_{p,c}w_c^2 + ck_{i,c}} \right) - \arctan\left(\frac{-ew_c^3 + gw_c}{dw_c^4 - fw_c^2} \right)$$

$$= -120°.$$

(2.75)

By rearrenging above equation and replacing the designed values

$$\left(\frac{-ak_{p,c}w_c^3 + bk_{i,c}w_c + ck_{p,c}w_c}{-ak_{i,c}w_c^2 - bk_{p,c}w_c^2 + ck_{i,c}} \right) = \tan\left(\arctan\left(\frac{-ew_c^3 + gw_c}{dw_c^4 - fw_c^2} \right) - 120° \right),$$

(2.76)

$$\left(\frac{2.3085e14k_{i,c} - 2.4830e17k_{p,c}}{-1.9769e13k_{i,c} - 2.8995e18k_{p,c}} \right) = -0.3635,$$

(2.77)

$$k_{i,c} = 5.8220e03k_{p,c}.$$

(2.78)

Substituting eq. (2.78) in eq. (2.74), the PI parameters for the current controller is reached

$$k_{i,c} = 227.9520,$$
$$k_{p,c} = 0.0392.$$

(2.79)

The bode diagram of the inner current PI controller is shown in Figure 2.21. The inner loop is satble with the cross-over frequency of $12560 rad/s$ and the phase margin of $60°$.
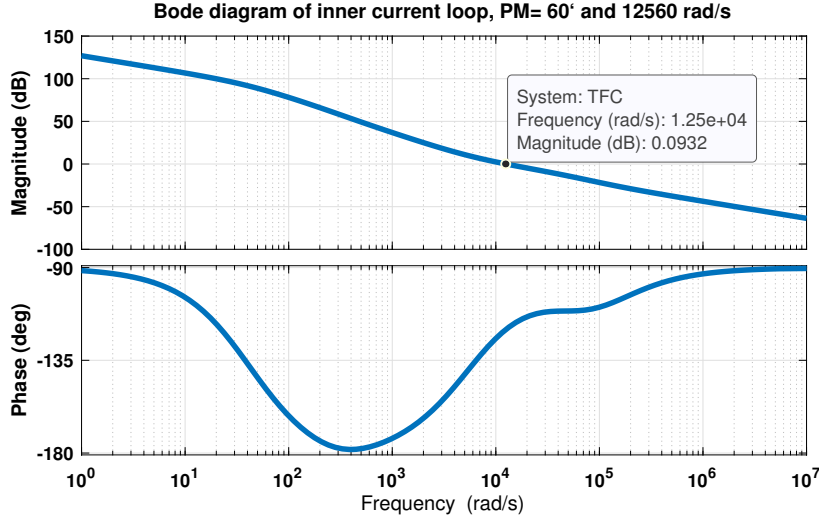
Figure 2.21: Bode diagram of inner current loop with PI controller in $w_c = 12560rad/s$.

2.5.2   Design of Voltage Control Loop

For the voltage loop transfer function, the boost inductor current to output voltage ratio is required eq. (2.80). The inner current control loop has faster dynamics compared to the outer voltage loop, correcting the current error according to the reference set by the voltage controller. The cross-over frequency for the voltage controller loop (w_v) is set to be at least one order lower than the cross-over frequency of the current controller. The transfer function of the inductor current to the output voltage for the the converter is

$$
\begin{aligned}
T_{p2} = \frac{\hat{v}_o}{\hat{i}_{in}} &= \frac{2(1 - D + D'')}{nC_o s + n/R_L}, \\
&= \frac{0.44}{0.0031s + 0.4}.
\end{aligned}
\tag{2.80}
$$

The open loop TF of voltage controller loop given by

$$
G_{OL,v} = T_{c2}.G_{OL,c}.T_{p2}.H_2,
\tag{2.81}
$$

where $G_{OL,c}$ is the gain of current loop which is designed in previous section to be 1, T_{c2} is the current PI controller transfer function, and H_2 is the voltage feedback gain, and assumed to be 1. For simplicity of the calculations, T_{p2} and T_{c2} are consider as below:

$$
T_{p2}(s) = \frac{a}{cs + b},
\tag{2.82}
$$

$$T_{c2}(s) = k_{p,v} + \frac{k_{i,v}}{s} = \frac{k_{p,v}s + k_{i,v}}{s}. \tag{2.83}$$

The open loop transfer function eq. (2.81) can be written as

$$\begin{aligned} G_{OL,v}(s) &= \left(\frac{a}{cs+b}\right) \cdot \left(\frac{k_{p,v}s + k_{i,v}}{s}\right), \\ &= \frac{ak_{p,v}s + ak_{i,v}}{cs^2 + bs}. \end{aligned} \tag{2.84}$$

The other form of above equation when $s = jw_v$ is

$$G_{OL,v}(jw_v) = \frac{ak_{i,v} + jak_{p,v}w_v}{-cw_v^2 + jbw_v}. \tag{2.85}$$

The conditions of designing PI controller is the same as current controller ($PM = 60°, |G_{OL}| = 1$). After testing different parameters for the voltage PI controller connected to the current controller, $75.4 rad/s$ is chosen as the gain of cross-over frequency among different values of cross-over frequencies. This cross-over frequency shows outer voltage loop is more than 100 times slower than the inner current loop.

$$\left|G_{OL,v}\right|_{s=jw_v} = \frac{\sqrt{(ak_{i,v})^2 + (ak_{p,v}w_v)^2}}{\sqrt{(-cw_v^2)^2 + (bw_v)^2}}. \tag{2.86}$$

By placing the known values the above equation changes to

$$\begin{aligned} \left|G_{OL,v}\right|_{s=j75} &= \sqrt{1.5867e - 04k_{i,v}^2 + 0.9020k_{p,v}^2}. \\ &= 1 \end{aligned} \tag{2.87}$$

The angle of the open loop transfer function of voltage controller is given

$$\begin{aligned} \angle G_{OL,v}\Big|_{s=jw_v} &= \arctan\left(\frac{k_{p,v}w_v}{k_{i,v}}\right) - \arctan\left(\frac{bw_v}{-cw_v^2}\right) \\ &= -120°. \end{aligned} \tag{2.88}$$

Rearrenging the above equation is

$$\left(\frac{k_{p,v}w_v}{k_{i,v}}\right) = \tan\left(\arctan\left(\frac{bw_v}{-cw_v^2}\right) - 120°\right). \tag{2.89}$$

$$k_{i,v} = 1.4434e4k_{p,v} \tag{2.90}$$

From eq. (2.87) and eq. (2.90) the PI voltage controller parameters can be found

$$\begin{aligned} k_{i,v} &= 79.3870, \\ k_{p,v} &= 0.0055. \end{aligned} \tag{2.91}$$

Figure 2.22 shows the bode diagram of voltage loop. The loop is stable in phase margin of $60°$ and the cross-over frequency of $75 rad/s$.
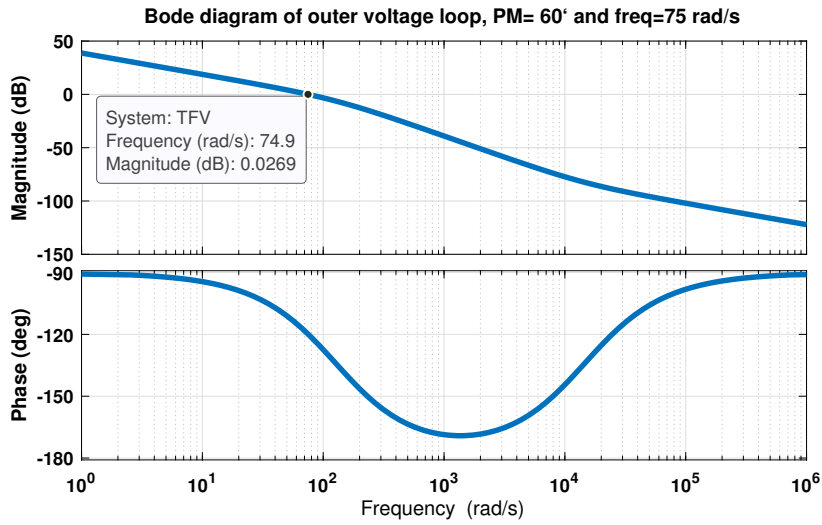
Figure 2.22: Bode diagram of outer voltage loop with PI controller in $w_v = 75 rad/s$.

2.5.3   Overall Transfer Function

The overall transfer function of the system can be written as

$$T_{OL}(s) = \left[\frac{T_{c1}(s).T_m(s).T_{p1}(s).H_1(s)}{1 + T_{c1}(s).T_m(s).T_{p1}(s).H_1(s)} \right].T_{c2}(s).T_{p2}(s).H_2(s). \qquad (2.92)$$

By substituting all parameters and PI controllers' TF calculated before, the open loop overall TF is:

$$T_{OL}(s) = \frac{15.8s^8 + 3.05e06s^7 + 1.664e11s^6 + 2.524e15s^5 + 1.068e19s^4 + 6.307e21s^3 + 1.1e24s^2 + 3.466e25s}{0.0031s^{10} + 407.6s^9 + 1.586e07s^8 + 1.704e11s^7 + 9.329e14s^6 + 6.707e17s^5 + 1.688e20s^4 + 1.565e22s^3 + 3.969e23s^2}$$

$$(2.93)$$

The bode plot for the overall system is drawn as shown in Figure 2.23. The gain at lower frequency is high which indicating zero steady state error. The phase margin of $60°$ at $75.4 rad/s$ is achieved resulting in a stable system against disturbances.

2.6   Loss Analysis

For the loss calculation of the current-fed full-bridge converter, the following simplifications are assumed:
1. The boost inductor is large enough and the input current i_{in} is well smoothed.
2. The output characteristic of the switches is modeled with the drain-source resistance $R_{DS,on}$.
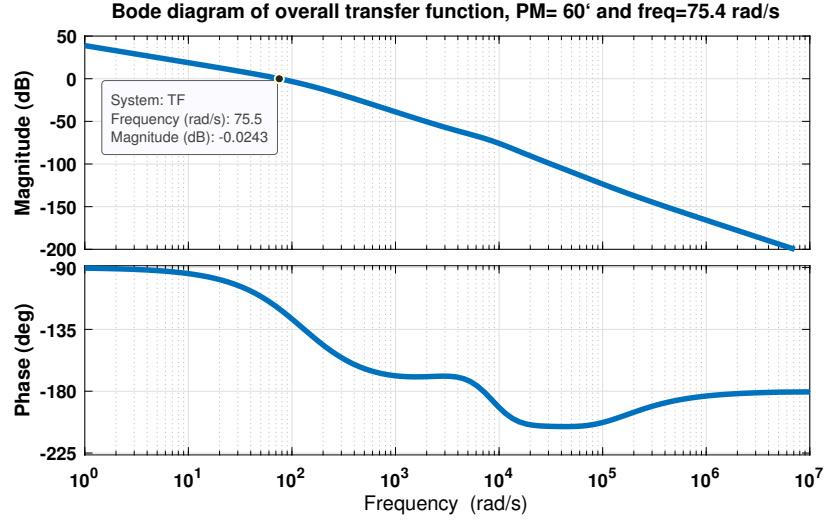
Figure 2.23: Bode diagram of control to output voltage TF with controller.

3. The output characteristic of the switch's body diodes and the rectifier diodes are modeled with a forward threshold voltage V_{F0} and a differential resistance r_F.

The switching losses of the body diodes and the rectifier diodes are calculated in [36], using their reverse recovery charge Q_{rr}, which depends on the slope of the falling diode current.

The switching losses of the diodes are comparatively low due to the slow current slopes. The switching losses are estimated by multiplying current and voltage waveforms (with rising time t_r and fall time t_f can be found in the respective datasheet) and integrating the product. As the transistor current rises very slowly, caused by the leakage inductance of the transformer, turn-on losses are zero (ZVS). But there are conduction and switching losses in the clamping diode [37]. The switch conduction loss is given

$$P_{con,mainS} = R_{DS,on} I_{in}^2 f_s \left[\left(\frac{2nI_{in}L_{lk}}{3V_o} \right) + \frac{1}{2} \left(\frac{D}{2f_s} - \frac{nI_{in}L_{lk}}{V_o} \right) \right] - R_{DS,on} I_{in}^2 f_s \left[\frac{2nI_{in}L_{lk}}{3(V_{Ca}-V_o/2)} + \frac{(1-D)}{2f_s} \right].$$
(2.94)

The switching losses is calculated

$$P_{sw,mainS} = f_s \left[\frac{V_o^2 t_r^2}{6n^2 L_{lk}} + \frac{V_{Ca} I_{in} t_f}{2} + \frac{I_{in} t_f}{4} \left(V_{Ca} + \frac{L_{lk} I_{in}}{2t_f} \right) \right].$$
(2.95)

Besides, the conduction losses of each of rectifier diode is given by

$$P_{con,RF} = f_s \left(V_{F0} \frac{I_{in}}{2n} + r_F \frac{I_{in}^2}{3n^2} \right) \left(\frac{I_{in}L_{lk}}{V_{Ca}-V_o/2} + \frac{nI_{in}L_{lk}}{v_o} \right) + f_s \left(V_{F0} \frac{I_{in}}{n} + r_F \frac{I_{in}^2}{n^2} \right) \left(\frac{(1-D)}{2f_s} - \frac{I_{in}L_{lk}}{V_{Ca}-V_o/2} \right).$$
(2.96)

The switching losses of one rectifier diode is

$$P_{sw,RF} = \frac{Q_{rr}V_o f_s}{4}. \tag{2.97}$$

The conduction and the switching losses of the clamping circuit are given by

$$P_{con,cl} = \frac{V_{F0}I_{in}^2 L_{lk} f_s}{V_{Ca} - V_o/2} + \frac{r_F I_{in}^3 L_{lk} f_s}{3(V_{Ca} - V_o/2)}, \tag{2.98}$$

$$P_{sw,cl} = Q_{rr} f_s (V_{Ca} - V_o/2). \tag{2.99}$$

2.7   Common-mode current

Since fuel cells have a wide variation in their output voltage from no load to full load, a power converter is required to interface the fuel cell connected to the utility. The power converter is usually constructed using a DC-DC converter (explained before for DC usage) connected in series with an inverter (for AC load). Both converters are normally operated by pulse width modulation (PWM). The operation of a power converter produces two types of outputs: a differential-mode (DM) voltage output and a common-mode (CM) voltage output [38]. The differential output is the output voltage of the system. On the other hand, the CM voltage is a voltage measured between the output lines of the converter and ground and the heat sinks of the power semiconductors or the transformers and the reference ground. Since the converter is operated using PWM, the CM output voltage has abrupt transitions to and from the DC bus voltage. These transitions induce large current spikes due to dV/dt across parasitic capacitances to ground throughout the whole circuit, Figure 2.24, [39]. These current spikes have large amplitude and short duration, and they are a function of the stray capacitances and the dV/dt of the CM voltage is rising and falling times. Power converters and inverters are enclosed in metal cabinets; thus, the current circulating through the ground generates most of the electromagnetic interference (EMI). This can also cause interference in the ground fault protection systems [38]. The effect of the CM noise induced by these currents on other components and equipment is a function of the distance separating the noise generation and reception. Therefore, it is important to keep the circulation paths of CM currents as short as possible.
The power converter in this paper contains an isolated DC-DC converter such as a full bridge, which is composed of an H-bridge inverter, a transformer, and a diode rectifier instead of a boost converter. In this topology, an equivalent circuit is obtained by modeling each inverter leg as a CM voltage source. The transformer in the DC-DC converter is modeled by capacitances from
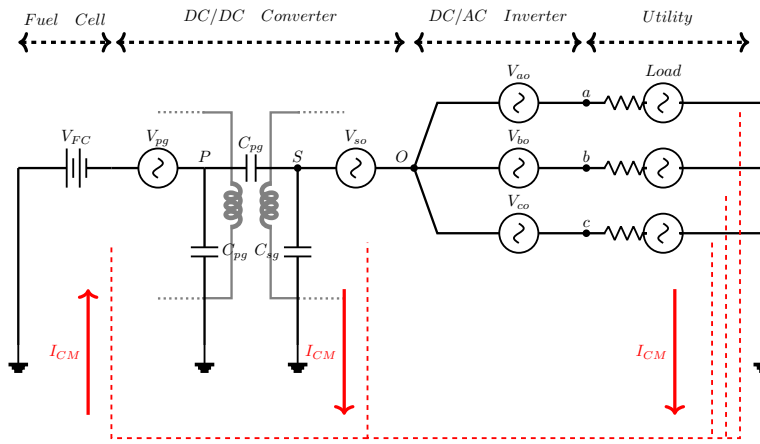
Figure 2.24: System parasitic capacitances and common-mode coupling paths.

primary and secondary to the ground (C_{pg},C_{sg}), which shows the distributed stray capacitances of each turn to the ground in both primary and secondary sides. An additional capacitance from secondary to primary (C_{ps}) models the parasitic capacitance between primary and secondary. Moreover, each leg in the three-phase inverter can be modeled as a switch-mode voltage source from the midpoint of the DC link "o" to one of the output lines of the inverter [40]. The CM current I_{cm} can then be calculated

$$I_{cm} = C_{ps} \frac{d(V_{og} + V_{so} - V_{pg})}{dt} + C_{pg} \frac{dV_{pg}}{dt}, \tag{2.100}$$

where V_{og} is voltage from point "o" to the ground and $V_{og} = \frac{V_{ao}+V_{bo}+V_{co}}{3}$. Moreover, V_{pg} and V_{so} are the CM voltages generated by the dc-dc converter and its rectifier. From Equation (2.100), the CM current can be reduced by reducing C_{ps}. A practical way of reducing the value of C_{ps} is by introducing a shield in the isolation transformer. The shield is then connected to ground and the capacitive coupling between the primary and the secondary is split and each part is connected to the ground. The final effect of this is breaking the circulation path for the CM current.

The CM current can further be reduced if a common-mode filter is connected at the output of the full-bridge. This can be accomplished by connecting a low-pass LRC filter between the inverter output terminals and the DC link, as shown in Figure 2.25. Also, the LRC filter can be designed to be located within the inverter. The two filter star points are electrically connected to the DC link's positive and negative points. The output filter neutrals to the DC link positive and negative points have advantages such as the symmetrical reduction of dV/dt at each switching transient. The peak amplitude of the CM current can be reduced if the rise and fall times of the CM voltage are increased. The
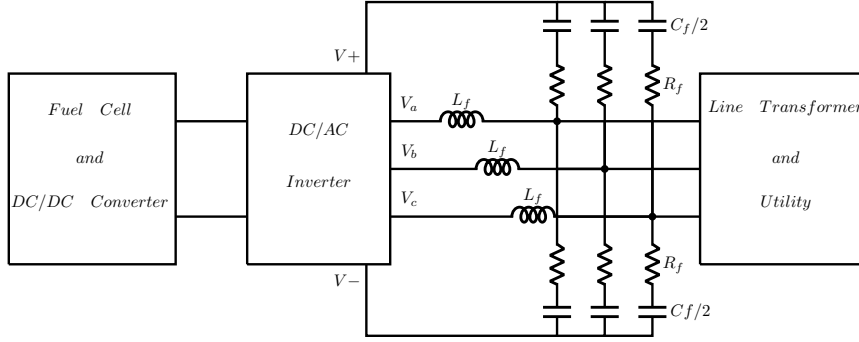
Figure 2.25: common-mode filter added to the topology.

common-mode voltage at the load terminals can be derived by

$$V_1 - V_{cm} = R_L i_{m1} \quad , \quad V_2 - V_{cm} = R_L i_{m2} \quad , \quad V_3 - V_{cm} = R_L i_{m3}, \quad (2.101)$$

where V_1, V_2, and V_3, are the load terminal voltages with respect to the ground and R_L is the per phase equivalent parameters of the load. Adding the three equations the following result is obtained.

$$(V_1 + V_2 + V_3) - 3V_{cm} = R_L(i_{m1} + i_{m2} + i_{m3}). \quad (2.102)$$

Since the common-mode current $i_{cm} \approx 0$, then $i_{m1} + i_{m2} + i_{m3} \approx 0$ and the below equation is obtained

$$V_{cm} = \frac{V_1 + V_2 + V_3}{3}. \quad (2.103)$$

The load terminal voltages can also be expressed as

$$V_1 = V_{1o} + V_{og} \quad , \quad V_2 = V_{2o} + V_{og} \quad , \quad V_3 = V_{3o} + V_{og}, \quad (2.104)$$

where V_{1o}, V_{2o}, and V_{3o} are the voltages between the load terminals and the DC link midpoint "o" and V_{og} is the voltage between the point "o" and the ground. The Equation (2.103) can be written as

$$V_{cm} = \frac{V_{1o} + V_{2o} + V_{3o}}{3} + V_{og}. \quad (2.105)$$

Figure 2.25 shows the load with the proposed output filter topology connected. The two filter star points are connected to the positive DC link bus bar and negative one. The below equation is driven for phase 1

$$V_{1o'} = R_f i_{o1+} + \frac{1}{C_f} \int i_{o1+} dt + V_{dc1} + R_f i_{o1-} + \frac{1}{C_f} \int i_{o1-} dt + V_{dc2}, \quad (2.106)$$

where R_f and C_f denote the values of filter. Since $V_{dc1} = -V_{dc2}$, then

$$V_{1o'} = R_f(i_{o1+} + i_{o1-}) + \frac{1}{C_f}\int (i_{o1+} + i_{o1-})dt \qquad (2.107)$$

It is easy to see that i_{o1+} and i_{o1-} are equal so

$$V_{1o'} = 2R_f i_{o1} + \frac{2}{C_f}\int i_{o1}dt. \qquad (2.108)$$

The same procedure is applied for the two other phases. As $i_o = i_{o1} + i_{o2} + i_{o3}$, the common-mode current is given

$$V_{cm} = \frac{V_{1o'} + V_{2o'} + V_{3o'}}{3} + V_{og} = \frac{2}{3}(R_f i_o + \frac{1}{C_f}\int i_o dt) + V_{og}. \qquad (2.109)$$

It can be concluded from Equation (2.109), that the common-mode voltage can be changed by designing properly the parameters of the proposed filter.
The peak amplitude of the CM current can be reduced if the rise and fall times of the CM voltage are increased. The mechanism of this filter is to reduce differential and common-mode by changing the rise time of the differential mode voltage pulses. The rise time can be increased on the voltage pulses by selecting the right time constant for the LRC filter. This critical rise time depends mainly on the length of the cable connecting the inverter and the load. For example, for a 30.48 $meters$ cable (100 ft) the critical rise time is about 2.5μsec [41]. The exponential equation of the inverter output voltage pulses when passed through the low pass LRC filter, is expressed in terms of the critical rise time, t_r as shown in Equation (2.110),

$$V(t) = V_{DC}(1 - e^{\frac{-t_r}{\tau}}), \qquad (2.110)$$

where τ is the time constant for the LRC filter and $\tau = \sqrt{L_f C_f}$. And, the rise time is calculated in a way to be smaller than time constant as

$$t_r \leq \sqrt{L_f C_f}. \qquad (2.111)$$

Furthermore, the critical value for capacitance is given by

$$C_r \geq l_{ca} * 151.2e - 12. \qquad (2.112)$$

Where l_{ca} is cable length in $[m]$. For instnace, for a cable length of 30m, the capacitance should be bigger or equal than 50nF and inductance value can be calculated 125μH from Equation (2.111). The resistance value is designed in order to obtain an over damped response:

$$R_f \geq \sqrt{\frac{4L_f}{C_f}} \qquad (2.113)$$

Then the resistor value results to be equal or higher than 100Ω. Using a shielded transformer and a common-mode filter practically eliminates the problem and reduce the CM current to the reasonable value.

/3

Simulation

3.1 Current-fed full-bridge converter (CFC) with the clamp circuit

The designed converter and controller are first simulated using MATLAB (R2021b) and Simscape, then built in the laboratory to verify the design, and performance of the converter. As explained in the chapter2, the duty cycle of main switches controls the output voltage of the converter. Based on the designing method, in the case of the minimum input voltage of $800V$, the duty cycle of 80% ensures the desired output of $1000V$. Besides, with the duty cycle of around 62% is the maximum input voltage of $1000V$, the same output voltage of $1000V$ is reached. The simulated converter without the controller is illustrated in appendix A. In this simulation two pulse generators are used to provide gate signals for switches.

The two legs of the converter's primary side are driven by the pulse with the frequency of $20k$Hz and a phase shift of $50°$, in a way that switches have some overlap. The other pulse of $40k$Hz with a duty cycle of 36% drives the auxiliary switch. A small phase shift is needed between main and auxiliary switches to ensure zero voltage switching (ZVS). The other parameters are listed in Table 2.1.

In the first test, $V_{in} = 800V$ and the duty cycle of main switches are set 80%. Figure 3.1 and Figure 3.2 show the waveforms of the designed circuit which coincide with the theoretical operating waveforms. When both of the main switches are on, i.e. $v_{AB} = 0$, current through the magnetizing inductance(i'_m)
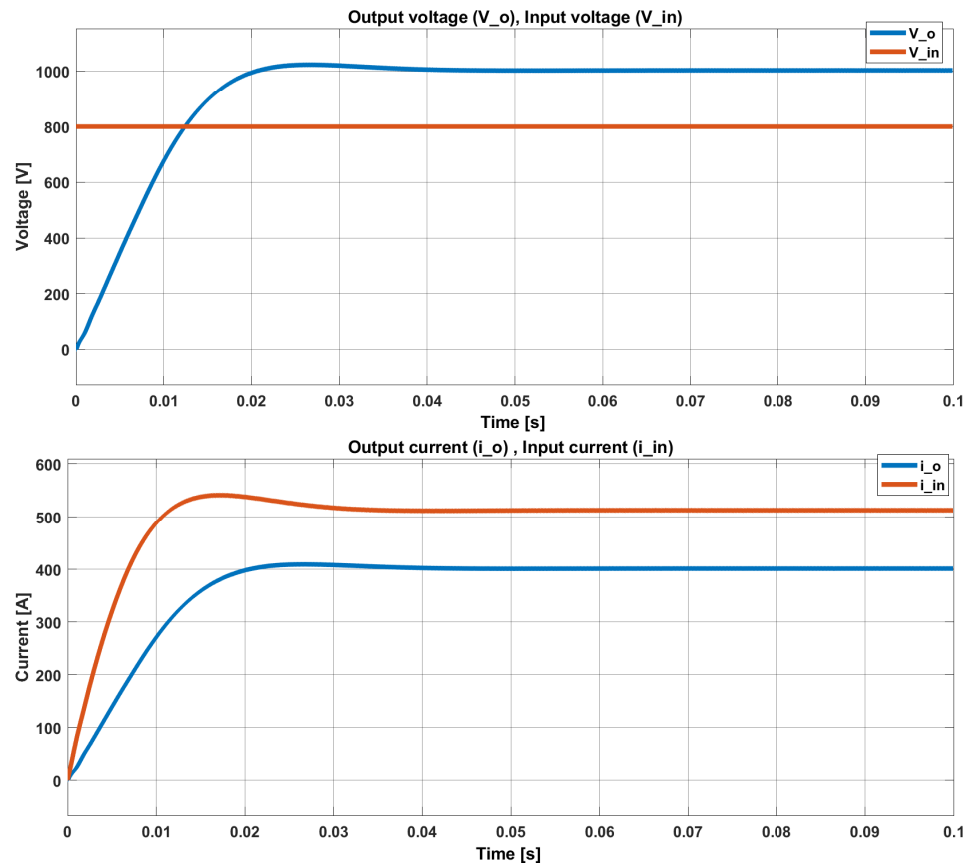
Figure 3.1: Input and output of CFC with clamp circuit, $V_{in} = 800V$ and $D = 0.8$.

is flowing through i_{lk} and are constant. Whenever one main switch is off, v_{AB} appears across the transformer and the current i_{lk} and i_m change direction. In the case of having a maximum input voltage of $1000V$, the duty cycle of 62% of main switches can ensure the output of $400kW$.

In the next test, input voltage is set to $1000V$ and the duty cycle of main switches are set 62%. Figure 3.3 and Figure 3.4 show the input and output voltage for this senraio under variety of the input signal shapes. At higher voltage, the duty cycle is low and therefore v_{AB} are non-zero for a longer time. It makes the currents i_{lk} and i_m to be constant for a very small duration and their shapes look triangular with a higher peak value compared to lower input voltage condition. It can be seen that the leakage inductance current i_{lk} is continuous due to the circulation of magnetizing current when all the main switches are on. It should be noticed that with an increase in input voltage or reduction in load current, the duty cycle of main switches reduces, which results in an increase in the peak value of magnetizing inductance current.
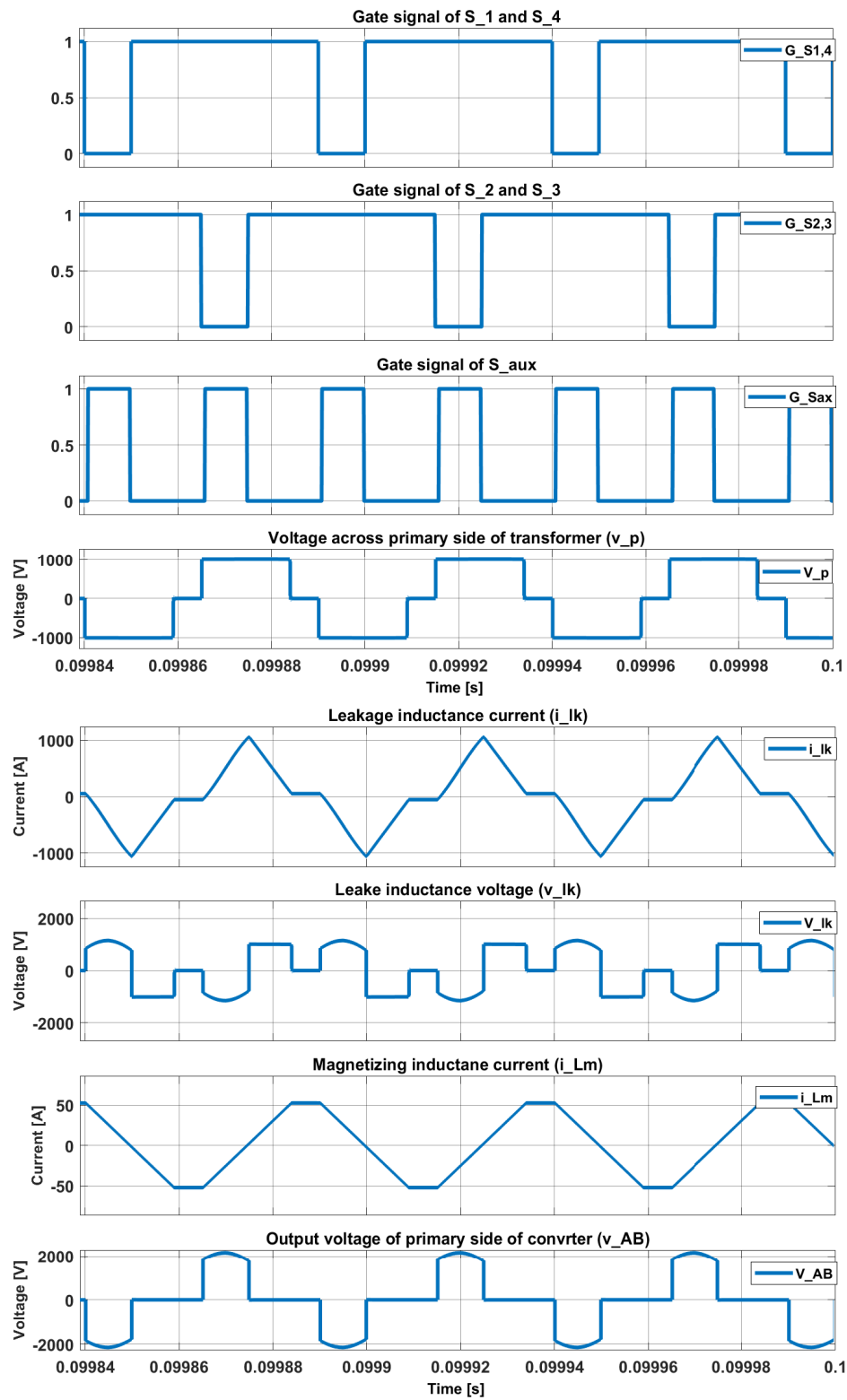
Figure 3.2: Simulation waveforms of CFC with clamp circuit, $V_{in} = 800V$ and $D = 0.8$.
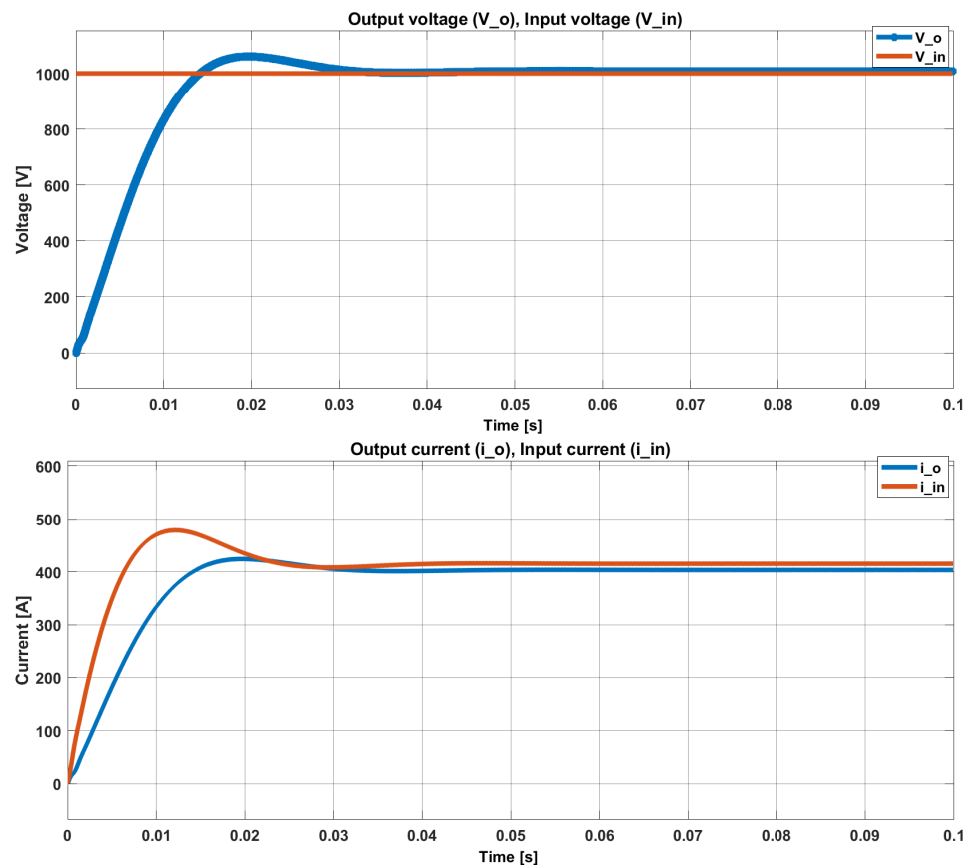
Figure 3.3: Input and output of CFC with clamp circuit, $V_{in} = 1000V$ and $D = 0.62$.

3.2   Current-fed full-bridge converter without clamp circuit

The effect of using the clamp circuit in choking overvoltage becomes quite clear while the simulation waveforms with and without the auxiliary circuit are compared. In Figure 3.5 the voltage across the leakage inductance and the main switch1 are shown. The over-voltage of around $84000V$ passes through switches and the leakage inductace which may damage switches and other elements in the circuit.
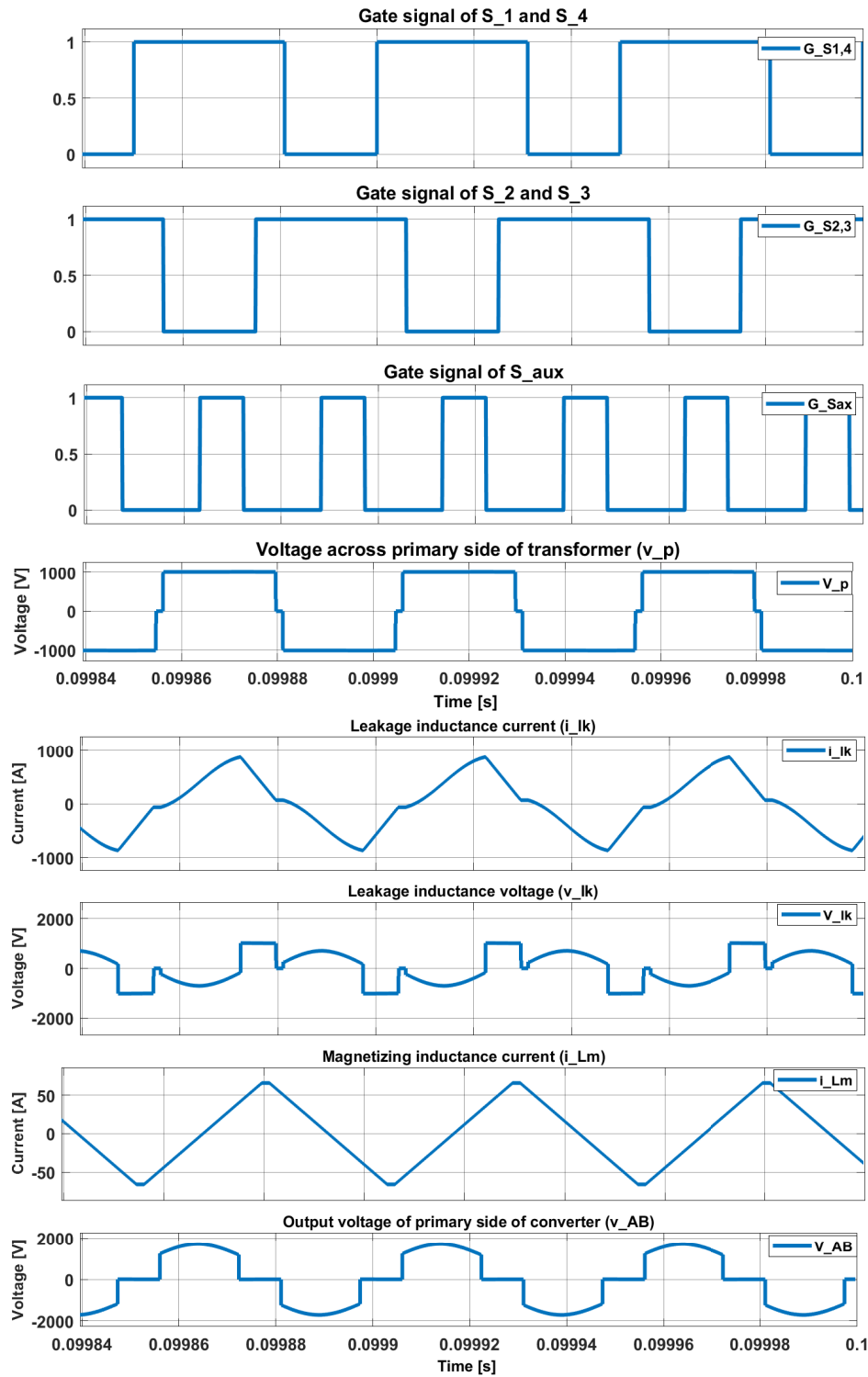
Figure 3.4: Simulation waveforms of CFC with clamp circuit, $V_{in} = 1000V$ and $D = 0.62$.

(a)

(b)
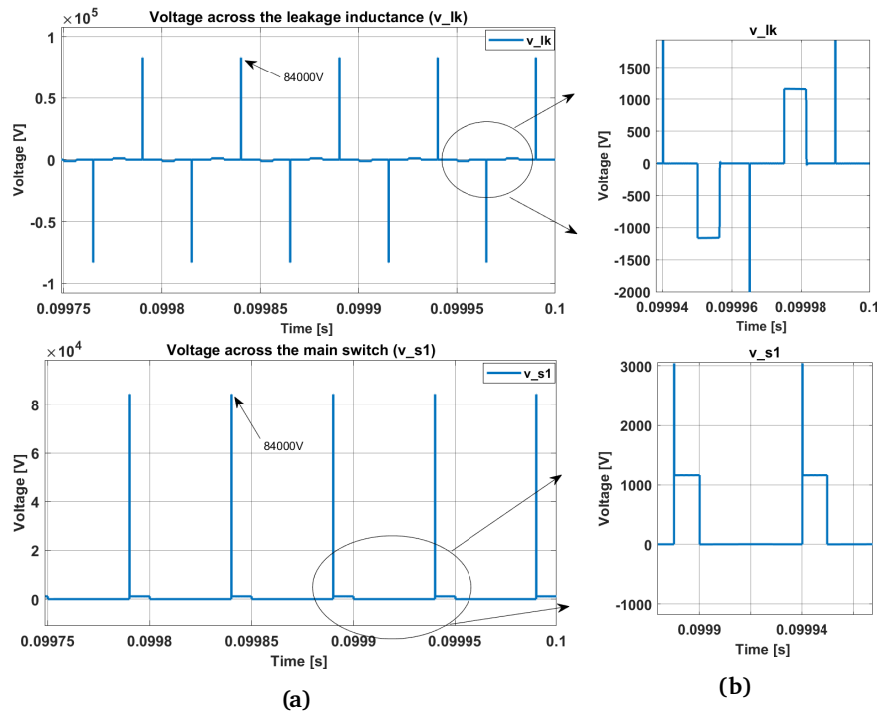
Figure 3.5: (a) Voltage across leakage inductance v_{lk} and the main switch1 v_{S1} of the converter without clamp circuit, $V_{in} = 800V$ and $D = 0.8$, (b) Closer look at the waveforms.

3.3 Current-fed full-bridge converter with the clamp circuit with controller

The controller's designed procedure is explained completely in Section 2.4 . Here, the controller block structure is discussed and added to the converter designed in the previous section.

The PI controllers parameters are listed in Table 3.1 and its block simulation is shown in Figure 3.6. The control blocks are added to the simulation of the

Table 3.1: Parameters of PI controllers' blocks(MATLAB simulation)

Outer voltage control loop		Inner current control loop	
Prameters	Value	Prameters	Value
$k_{i,v}$	79.38	$k_{i,c}$	227.9520
$k_{p,v}$	0.0055	$k_{p,c}$	0.0392

converter with two additional sensors. The output voltage of the converter, measured by a sensor, acts as an input to the outer voltage control loop along with a reference voltage. The voltage control loop provides the reference signal for the input inductor current. This signal plus measured boost inductor current,
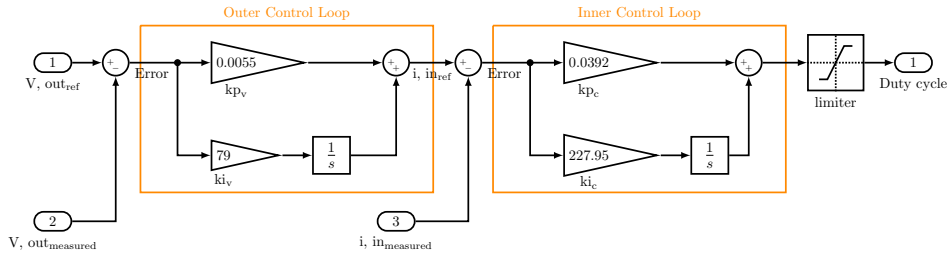
Figure 3.6: CFC PI controllers' block with outer and inner control loop.
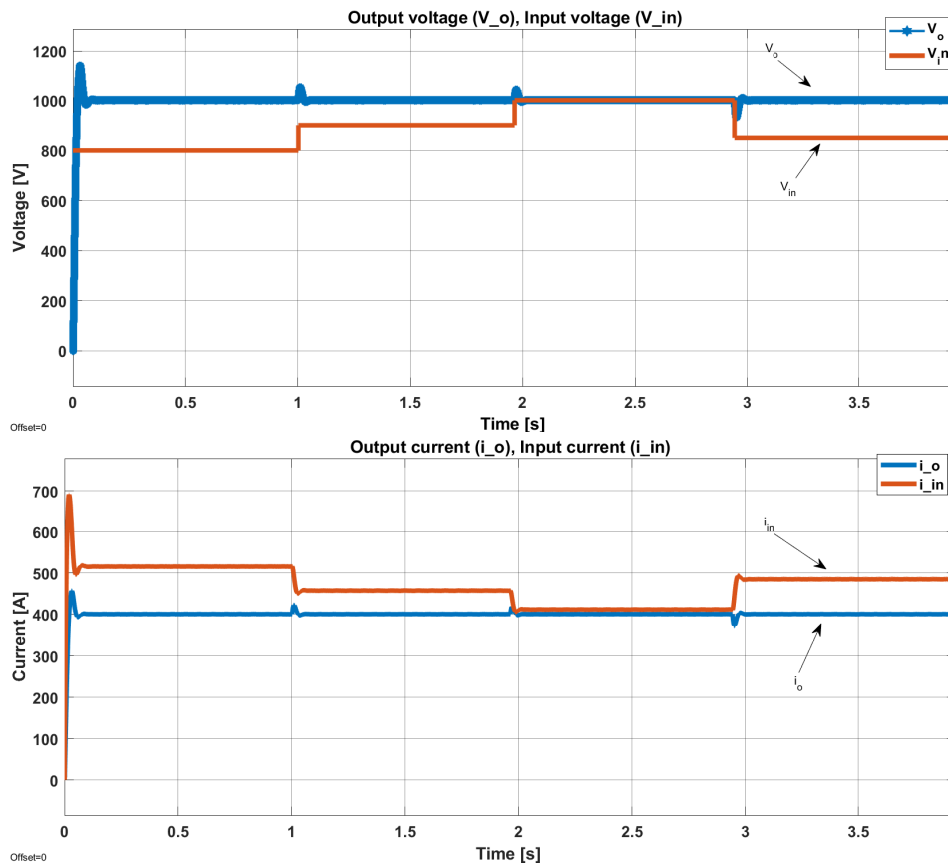
Figure 3.7: Response of converter to varied input voltage, MATLAB simulation.

are input to the inner control loop, which provides a reference duty cycle for main switches. Moreover, there is a need for a PWM generator block to create a pulse according to the reference duty cycle.

The simulation of the converter with controller is shown in appendix B. The output voltage reaches the reference voltage regarless the input voltage value (the system is designed in a way that the input voltage can not be lower than $800V$). Figure 3.7 plots the converter's output voltage under the sudden change of the input voltage from $800V$ to $1000V$. This sudden input voltage change will cause the output voltage waveform to jump sharply to adapt to the new input voltage and stabalizes.

Simscape simulations enables a smoother input variation and a better look into the functionality if the desined controller in reality. Therefore, the whole system with some minor modification is simulated in Simscape as shown in appendix C.

The controller subsystem is triggered with the same frequency as the main switching frequency of $20k$Hz. Besides, the continuous integrators are replaced with discontinuous ones. As it can be seen in Figure 3.8, output voltage and current are almost constant when input voltage changes from $800V$ to $1000V$. The sudden changes in output,due to variation in input voltage, is smoother when input changes are not sharp and instance.

Figure 3.9 depicts the efficiency of the transformer as the output (isn't load always output) load varies. As can be seen, over $P_{out} = 400kW$ and lower than $P_{out} = 300kW$, the efficiency of the converter and controller drops. The efficiency in $P_{out} = 400kW$ is about 97% in both minimum and maximum input voltage cases.

3.4   Zero Voltage Switching

Active clamp circuits can be used to absorb the resonant leakage energy and recover it to the load side whilst clamping the voltage across the main switching devices [3]. This has the additional advantage of operating the main switches with ZVS at turn-on, thus improving converter efficiency.

The gate-source and drain-source voltages of the main switch1 are shown in Figure 3.10. Gating signals are applied to the main switches after the voltage across them reaches zero. The ZVS in off and on-states of main switches is also confirmed since the anti-parallel diode is conducting before the switch starts conducting. The voltages across the auxiliary switch and its gate signal are shown in Figure 3.11. The auxiliary switch is gated for ZVS during turn-on, but losses during off-state are noticeable.
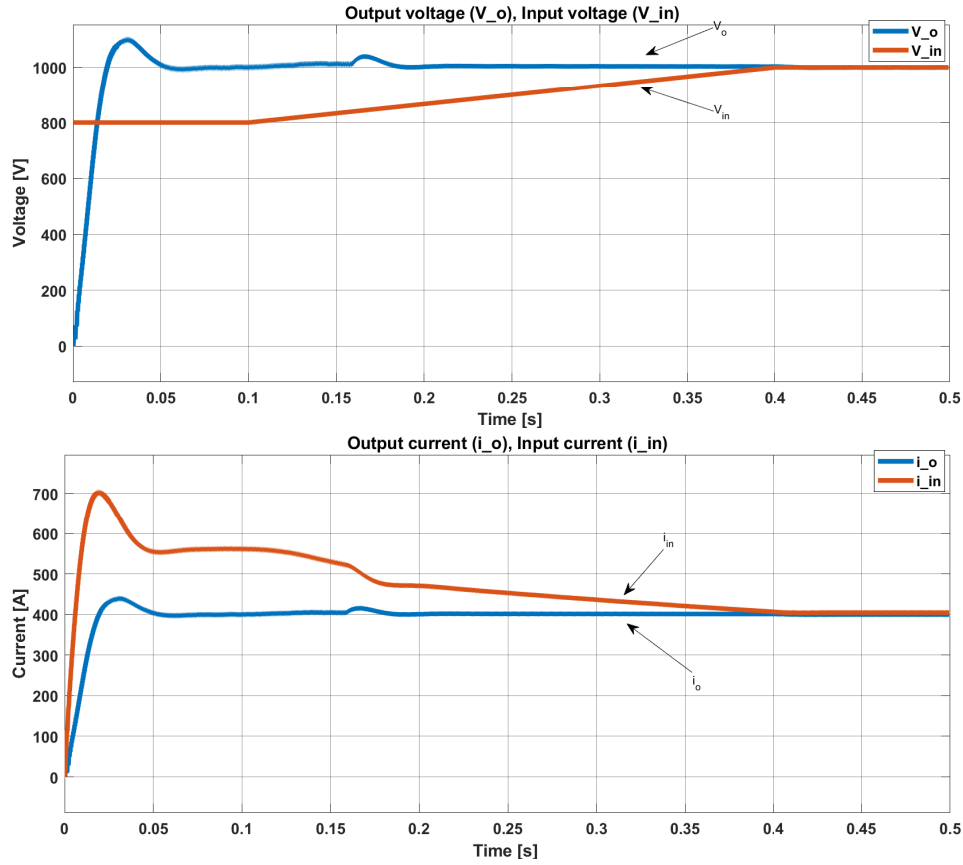
Figure 3.8: Response of converter to varied input voltage, Simscape simulation.
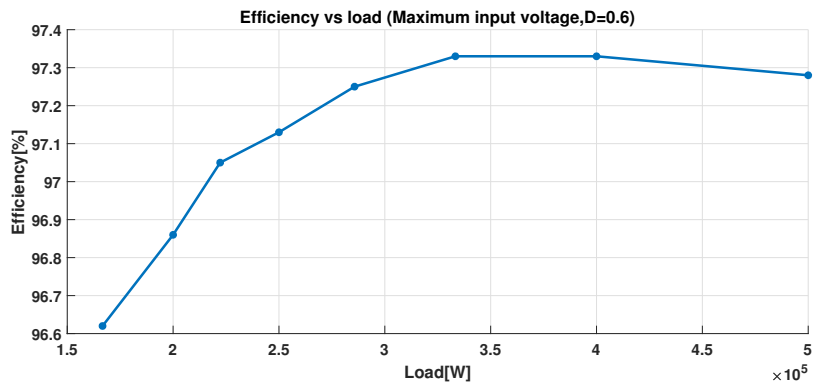
Figure 3.9: Efficiency of circuit regards to output load, $V_{in} = 1000V, D = 0.6$.
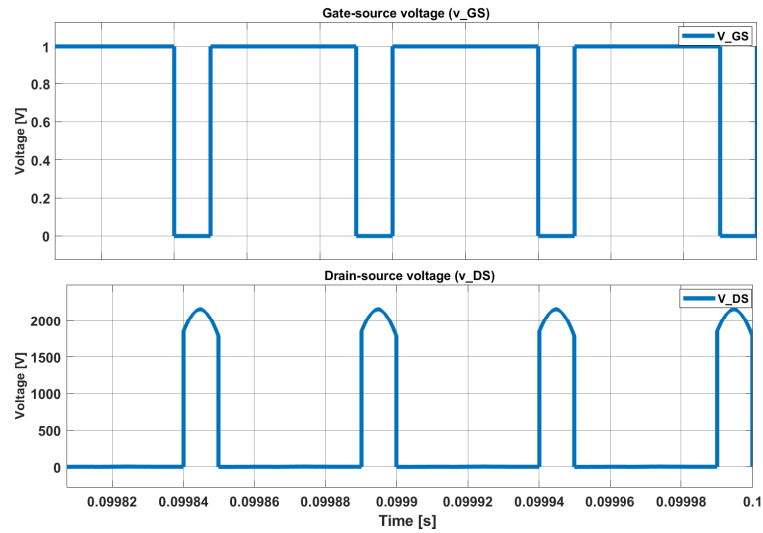
(a)
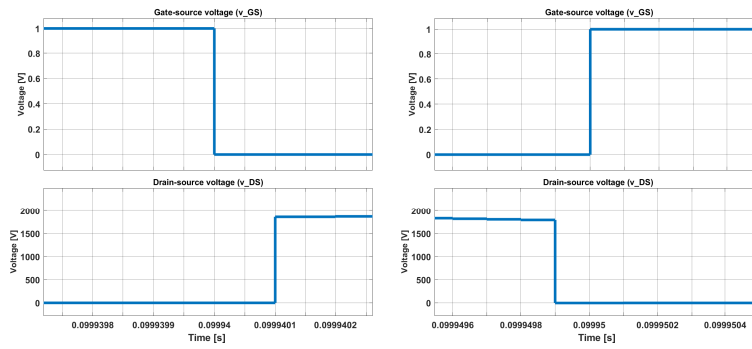
(b)

(c)

Figure 3.10: (a) Gate-source, drain-source voltages across the main switch1, $V_{in} = 800V$ and $D = 0.8$, (b) ZVS in Off-state, (c) ZVS in On-state.
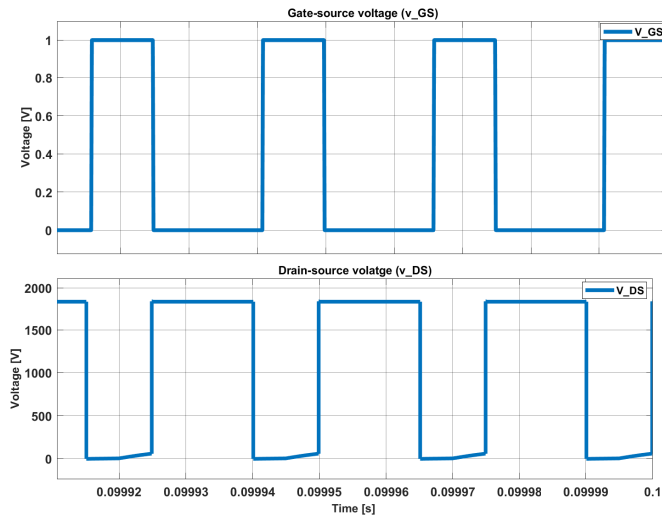
(a)
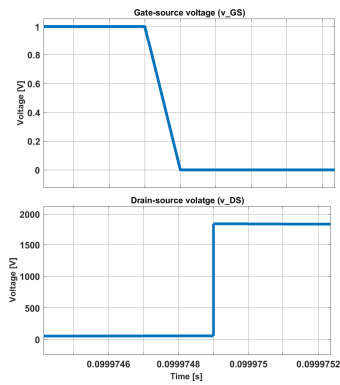
(b)
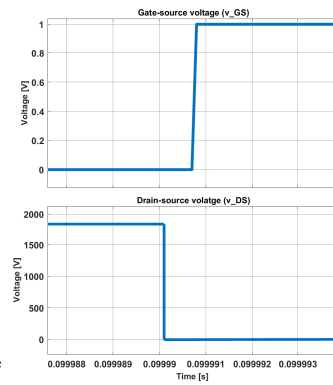
(c)

Figure 3.11: (a) Gate-source, drain-source voltages across the auxiliary switch, $V_{in} = 800V$ and $D = 0.8$, (b) losses during Off-state, (c) ZVS in On-state.

3.5   Fast Fourier Transform analysis

A Fast Fourier Transform (FFT) analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain and vice versa. In a complex signal, the FFT helps to determine the frequencies that are being excited in the signal and the amplitude at each frequency. When the frequency components of the signal is driven out, it is easier to view changes in frequency and amplitude in a waveform and highlight harmonic excitation. FFT analysis is done for simulation and the result is shown in Figure 3.12. The strength of the fundumental frequency components of $20k$Hz is higher than the other components because all elements are considered to be ideal and no noise sources or leakages exist in the simulation model.
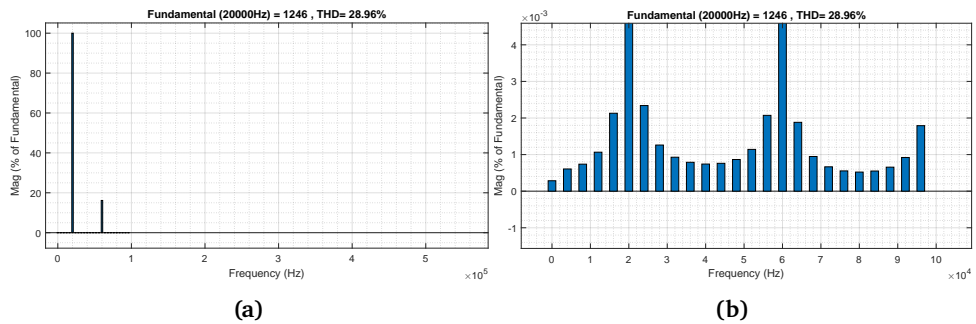
Figure 3.12: (a) FFT analysis, (b) The closer look at harmonics.

4

Experimental Results

4.1 Design of Experimental Model

4.1.1 Converter Design

An experimental prototype is done based on the scaled value in the laboratory. Because of equipment limitations, the desired voltage output is scaled to $20V$ and $20W$ output power, while the input voltage varies between $12V$ and $20V$. The method is the same as that explained in chapter2, but with new assumptions. The MATLAB m-files for designing the convereter, transformer, and controller are attached in appendix D. The assumptions and designed values are listed in Table 4.1 and Table 4.2, respectively.

Table 4.1: Assumptions of Lab Experimental Design.

Specifications	Symbol	values	Specifications	Symbol	values
Input voltage	V_{in}	$12-20V$	Maximum duty cycle of main switches	D_{max}	0.8
Output voltage	V_o	$20V$	Boost inductor ripple current	Δi_{in}	$0.1A$
Output power	P_o	$20W$	Ripple in output voltagle	Δv_o	$0.1V$
Load resistance	R_L	20Ω	Ripple in auxiliary capacitor voltage	Δv_{Ca}	$1V$
Transformer turn ratio	n	1	Inductance ratio	L'_m/L_{lk}	30
Main switching frequency	f_s	$20kHz$	Auxiliary switching frequency	f_s	$40kHz$

Table 4.2: Values of the Parameters Obtained from Designed Equations for Lab Experiment.

Specifications	Symbol	values	Specifications	Symbol	values
Input inductor	L	$0.6mH$	Auxiliary capacitor	C_a	$3.6\mu F$
Leakage inductor	L_{lk}	$12\mu H$	Auxiliary switch capacitor	C_{ax}	$5nF$
Magnetizing inductor	L_m	$1.45mH$	Output capacitor	C_o	$1mF$

4.1.2 Transformer Design

Normally, for high switching frequency applications, ferrite cores should be selected to eliminate eddy current loss in the core. The ferrite ETD 39/20/13 is chosen for this matter and its specification is listed in Table 4.3. The data sheet of the core can be found in appendix E. The copper wire $AWG14$ with inner and outer diameter of $d_i = d_o = 1.62mm$ is also selected due to hight current passing through the circuit. The Area Product method (AP) of designing a

Table 4.3: Ferrite Core Data; ETD39/20/13.

Specifications	Symbol	values	Specifications	Symbol	values
Effective magnetic cross section	A_c	$125mm^2$	Winding area	A_a	$177mm^2$
Effective magnetic path length	l_c	$92.2mm$	Saturation flux density	B_s	$0.32T$
Effective magnetic volume	V_c	$11500mm^3$	Rlative effective permeability	μ_a	1650

transformer for the converter is presented in [42]. This method involves core material selection, core and wire shape, size, and allocating of core window area. Moreover, it provides all values of transformer, losses, temperature rise, efficiency and etc. Only the relevant part of the transformer design process is discussed in this section.

Here, it is assumed that the current density of wire is $J_m = 5A/cm^2$ and core window utilization factor is $K_u = 0.3$. The cross-sectional area of the primary winding is calculated by

$$A_{wp} = \frac{i_{in,max}}{J_m}. \tag{4.1}$$

The number of strands in primary winding is given by

$$S_p = \frac{A_{wp}}{A_{wst}}, \tag{4.2}$$

where A_{wst} is the cross section area of chosen wire, and is equal to $(\pi d_i^2)/4 = 2.08mm^2$. The value of S_p is rounded up to 1. The number of turns of primary winding can be calculated as

$$N_p = \frac{K_u W_{ap}}{S_p A_{wpo}}, \tag{4.3}$$

where W_{ap} is the area allocated to the primary winding and equals to the core window area here. The cross-section area of insulated strand wire, i.e. A_{wpo}, is

Table 4.4: Open Circuit Test.

Measuring primary side's parameters			
Equipment	**Frequency**	**Magnetizing Inductance**	**Parallel Resistance**
LCR Meter E-1242	1 kHz	1.484 mH	1.20 $k\Omega$
LCR Meter E-1242	10 kHz	1.472 mH	16.10 $k\Omega$
LCR Meter E-1242	100 kHz	1.505 mH	140.90 $k\Omega$
HEWLETT PACKARD 4285A	75 kHz	1.460 mH	180 $k\Omega$
Calculated value	20 kHz	1.475 mH	30.2 $k\Omega$
Measuring secondary side's parameters			
Equipment	**Frequency**	**Magnetizing Inductance**	**Parallel Resistance**
LCR Meter E-1242	1 kHz	1.485 mH	1.18 $k\Omega$
LCR Meter E-1242	10 kHz	1.470 mH	16.30 $k\Omega$
LCR Meter E-1242	100 kHz	1.498 mH	147.5 $k\Omega$
HEWLETT PACKARD 4285A	75 kHz	1.460 mH	180 $k\Omega$
Calculated value	20 kHz	1.473 mH	30.8 $k\Omega$

Table 4.5: Short Circuit Test.

Measuring primary side's parameters			
Equipment	**Frequency**	**Leakge Inductance**	**Series Resistance**
LCR Meter E-1242	1 kHz	6 μH	0.075 Ω
LCR Meter E-1242	10 kHz	5.38 μH	1.18 Ω
LCR Meter E-1242	100 kHz	3.406 μH	9.70 Ω
HEWLETT PACKARD 4285A	75 kHz	3.480 μH	0.379 Ω
Calculated value	20 kHz	5.16 μH	2.13 Ω
Measuring secondary side's parameters			
Equipment	**Frequency**	**Leakge Inductance**	**Series Resistance**
LCR Meter E-1242	1 kHz	6 μH	0.075 Ω
LCR Meter E-1242	10 kHz	5.36 μH	1.17 Ω
LCR Meter E-1242	100 kHz	3.395 μH	9.62 Ω
HEWLETT PACKARD 4285A	75 kHz	3.495 μH	0.379 Ω
Calculated value	20 kHz	5.14 μH	2.11 Ω

the same as A_{wst} and equals to $2.08mm^2$. In above equation, number of turns in primary side of the transformer is reached $N_p = 26$. As the transformer turn ratio is one, then both sides have the same number of turns.

The designed transformer is built and the short and open circuit tests are applied to measure the leakage inductances, magnetizing inductances and resistances values. Both experiments are conducted on two (independent trials). The results of these experiments can be found in Table 4.4 and Table 4.5 . The used equipement has some limitations in working frequencies. The transformer's parameters in the frequency of $20k$Hz are calculated by assuming parameters' variation between $10k$Hz and $100k$Hz are linear.

4.1.3   Leakage Inductance Design

The value of leakage inductance, which is needed to transfer power from primary to secondary side, L_{lk}, is $12\mu H$ based on the Table 4.2. On the other hand, the leakage inductance of the primary and the secondary sides of transformer is around $5\mu H$, which is $11.3\mu H$ in total. Then, there is no need for an extra inductor to be placed in series with the transformer.

4.1.4   Controllers Design

Inner Current Controller:
The method applied for the controller is the same as explained in Section 2.4. The boost inductor current to the duty cycle transfer function of the current loop is obtained given by

$$T_{p1} = \frac{\hat{i}_{in}(s)}{\hat{d}(s)} = \frac{3e4s^2 + 3.149e8s + 5.896e10}{s^3 + 9386s^2 + 5.62e6s + 1.379e9}.$$ (4.4)

The 2 criteria for designing the PI controllers,$(\left|G_{OL,c}\right|_{s=jw_c} = 1$ and $\angle G_{OL,c}\big|_{s=jw_c} = -\pi + PM)$, is applied to the above transfer function. With the cross-over frequency of $1256rad/s$ and phase margin of $60°$, two equations of eq. (4.5) and eq. (4.6) are achieved. By solving these equations, the PI parameters for the inner current loop are found.

$$\sqrt{4.8159e - 4k_{i,c}^2 + 759.7246k_{p,c}^2} = 1,$$ (4.5)

$$\left(\frac{2.3085e14k_{i,c} - 2.4830e17k_{p,c}}{-1.9769e13k_{i,c} - 2.8995e18k_{p,c}}\right) = -0.3635.$$ (4.6)

Outer Voltage Controller:
For the outer voltage loop, the boost inductor current to output voltage transfer

function is given

$$T_{p2} = \frac{\hat{v}_o}{\hat{i}_{in}} = \frac{0.44}{0.001s + 0.05}. \tag{4.7}$$

With the same criteria and cross-over frequency of $125.6\,rad/s$, two below equations are reached.

$$\sqrt{6.7025e - 4k_{i,v}^2 + 10.5842k_{p,v}^2} = 1, \tag{4.8}$$

$$k_{i,v} = 159.1006k_{p,v}. \tag{4.9}$$

The parameters for PI controllers are listed in Table 4.6. The overall transfer

Table 4.6: Parameters of PI controllers' blocks (Experimental Design).

Outer voltage control loop		Inner current control loop	
Prameters	Value	Prameters	Value
$k_{i,v}$	30.3115	$k_{i,c}$	34.4053
$k_{p,v}$	0.1905	$k_{p,c}$	0.0238

function of the system and its bode diagram are shown in eq. (4.10) and Figure 4.1. As it can be seen, the overall transfer function is stable in the phase margin of 59 degrees and frequency of $125\,rad/s$.

$$T_{OL}(s) = \frac{755.2s^8 + 2.721e7s^7 + 2.926e11s^6 + 1.015e15s^5 + 1.5e18s^4 + 9.989e20s^3 + 2.802e23s^2 + 2.472e25s}{0.001s^{10} + 38.5s^9 + 6.094e5s^8 + 4.501e9s^7 + 1.345e13s^6 + 1.791e16s^5 + 1.053e19s^4 + 2.337e21s^3 + 9.269e22s^2}. \tag{4.10}$$

4.2 Experimental Model

An experimental prototype is built for the specifications and design given in the above section. For the primary switch side of converter, an Intelligent Power Modules (IPM) from Mitsubishi Electric company along with its external evaluation board is used. IPMs are advanced hybrid power devices that combine high-speed, low-loss Insulated-Gate Bipolar Transistors (IGBT) with optimized gate drive and protection circuitry. The IPM50RSA120 is based on a 3-phase inverter circuit and contains 7 IGBTs but only 4 of them are used as converter parts of the circuit. This module is a $1200V$ and $50A$, and the perfect device for testing the system without the clamp circuit. The data sheet of the IPM and its external evaluation board are attached in appendix F.

The evaluation board needs an input voltage of $24V$ for driving the IPM, and a supplier of maximum $42V$ and $5A$ (maximum power of $320W$) provides the input for it. The diode bridge with $300V$ and $20A$ is placed as the secondary
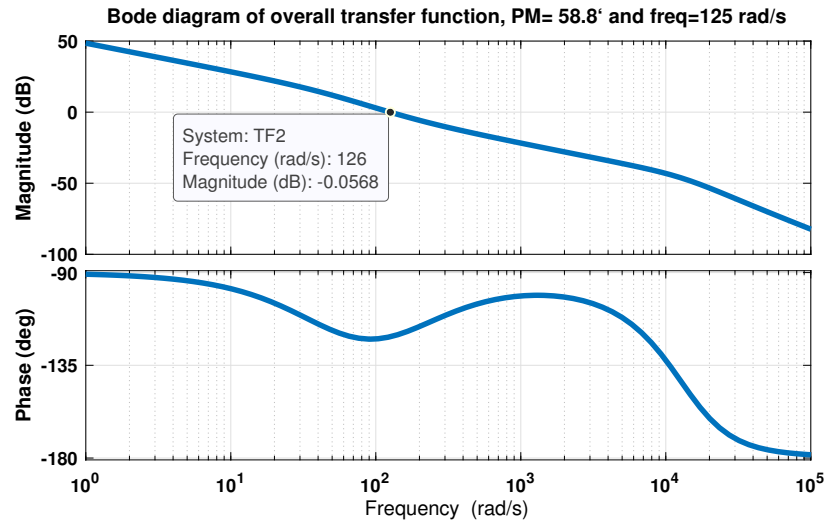
Figure 4.1: Bode diagram of control to output voltage transfer function with controller(Experimental Design).

inverter side. Two variable resistors with maximum 10Ω and $7A$ are used in series as load.

First Step:
The circuit is built without the auxiliary clamp switch and controller. For driving the IPM, two pulses with overlap are needed. As a pulse generator can only produce sine waves with overlap (not square waves), the required pulses are generated by dSPACE setup (ControlDesk software and MicroLabBox). Two square waves with a frequency of $20k$Hz and phase shift of 60 degrees are generated and connected to the pins of the evaluation board.
Another supplier with similar specifications mentioned before provides the input voltage of the converter and is connected to the IPM through the boost inductor of $2mH$. The two pins "W" and "U" of IPM which are the output of the primary side of the converter, are connected to one side of the designed transformer The secondary side of the transformer is connected to the output capacitor of $1mF,40V$ and load resistors through the diode bridge, see Figure 4.2.
The Figure 4.3 shows the boost inductor current and the voltage across the secondary side of the transformer when input voltage (V_{in}) is around the maximum designed value $20V$ and duty cycle of gate signals are 62% (The data are collected from an oscilloscope and plotted in MATLAB).
In the case of minimum input voltage $V_{in} = 12V$, the duty cycle of main switches must be around 80% in order to have $20V$ as the output voltage. However, the input voltage has not been increased more than $V_{in} = 9.95V$

when $D_{max} = 80\%$ due to a huge voltage spike over elements. The Figure 4.4 shows the waveforms in this case. The maximum and minimum voltages across the transformer in both situations are $63V$ and $-80V$. The V_{in} shouldn't be increased more before adding clamp circuit in order to omit this overvoltage.
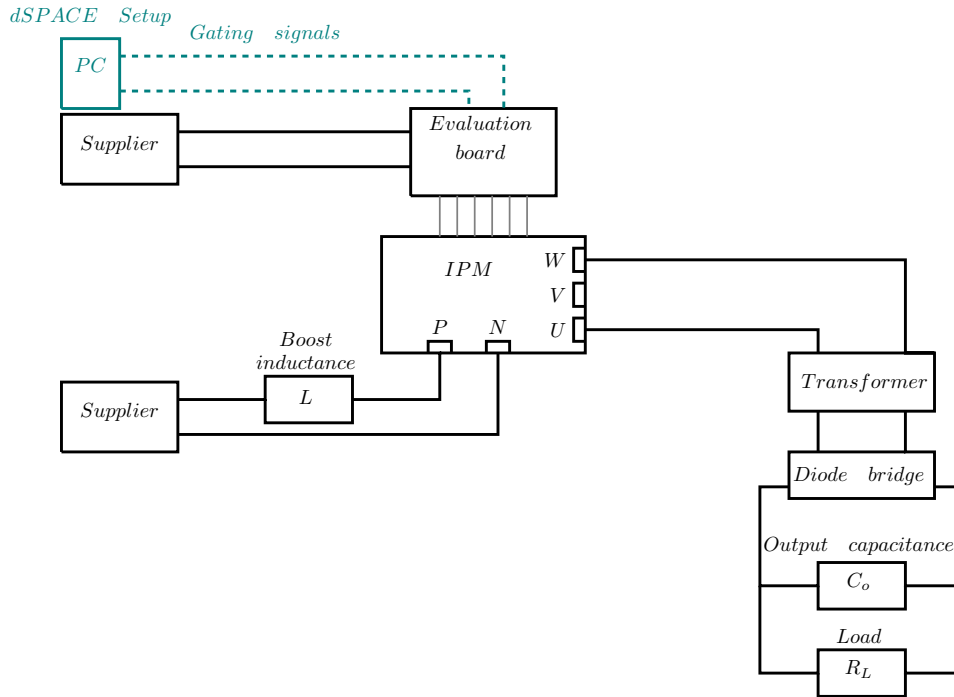
Figure 4.2: Schematic of the physical circuit, converter without clamp circuit and controller.

Second Step:
For the auxiliary switch of the clamp circuit, another IPM module and evaluation board are used. One capacitor C_{ax}, in parallel with the switch of IPM, and another auxiliary capacitor C_a in series with this switch are added to the circuit. For driving the IPM, another square wave with a frequency of $40k$Hz and a duty cycle of 20% is generated by dSPACE. The schematic of the converter with clamp circuit is depicted in Figure 4.5. The auxiliary switch turns on whenever each leg of the main converter turns off with a small delay. The Figure 4.6 and Figure 4.7 show the boost inductor current and voltage across the secondary side of the transformer after adding the clamp circuit in minimum and maximum input voltage situations.

In presence of the clamp circuit, the huge voltage spike over elements is almost removed and it is feasible to reach higher output voltage without damaging elements. The voltages across the transformer fluctuate between $22V$ and $-28V$ in minimum input voltage, and between $37V$ and $-45V$ in maximum
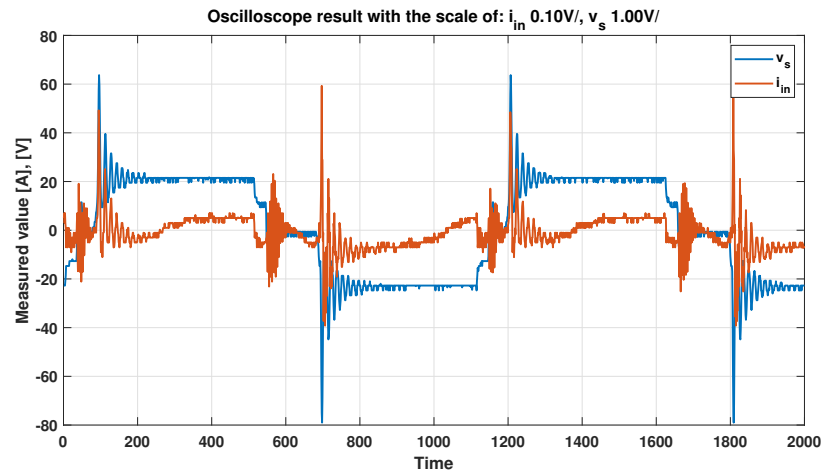
Figure 4.3: Input boost current and secondary side transformer voltage without clamp circuit, $V_{in} = 19.95V$, $D = 0.6$.
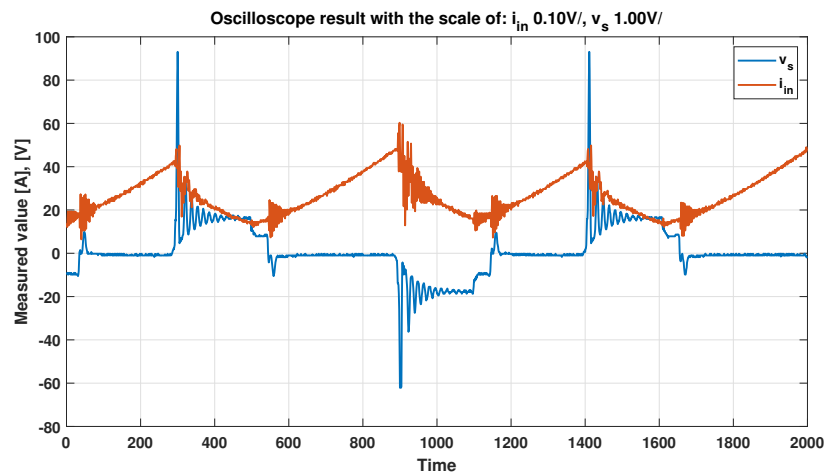
Figure 4.4: Input boost current and secondary side transformer voltage without clamp circuit, $V_{in} = 9.95V$, $D = 0.8$.

input. Moreover, the efficiency of the system increases slightly in low input voltage cases(higher duty cycles). The output results of the two above steps are listed in Table 4.7 and Table 4.8. In the next step, the controller is added to the system.
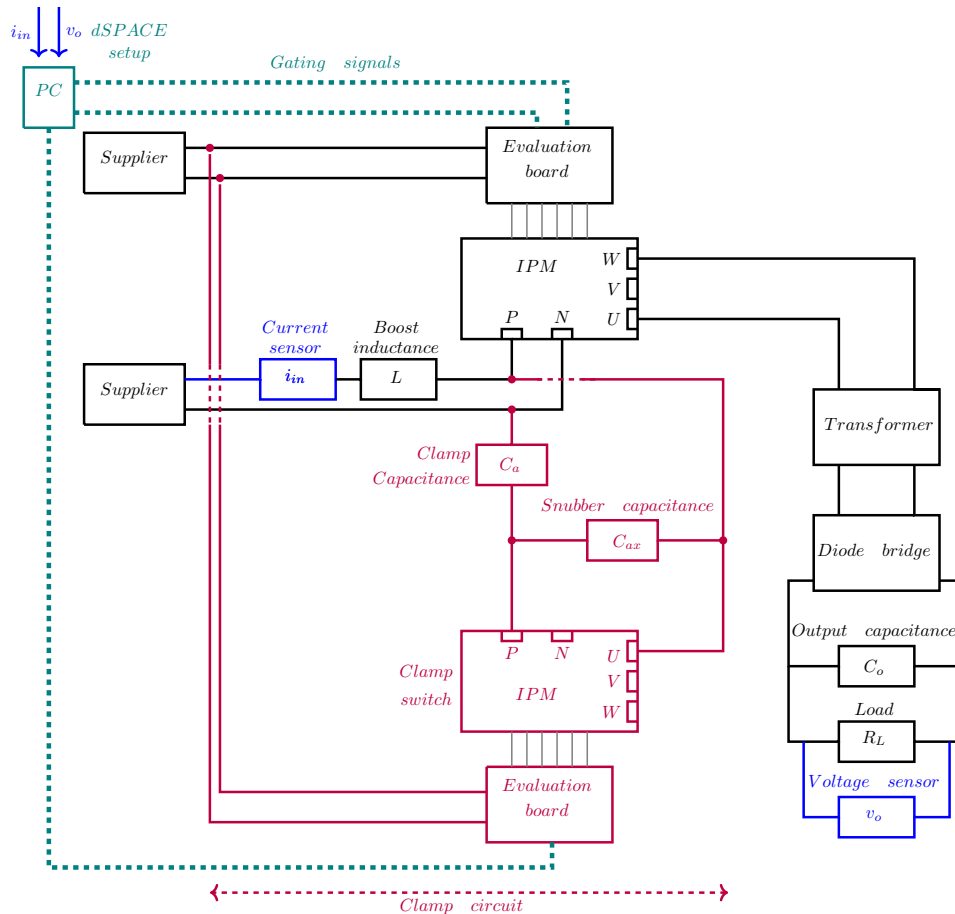
Figure 4.5: Scematic of the physical circuit, converter with clamp circuit.

Last Step:

In controller design, a real-time system requires more start-up procedures in order to prevent any damage to the system. A reset function is added to the PI controllers to reset the integrator and ensure zero output as long as the reset input is zero. Following Figure 4.8 and Figure 4.9 are shown outer voltage and inner current PI controllers, with improved anti-windup. The absolute block can stop the integrator if the output absolute value goes above the given current limit. One current sensor with the gain of 1 measures the boost inductor current and is connected to the dSPACE through the pin $Al1ch2$. Also, one voltage sensor with the gain of 1/50 transfers the measured output voltage
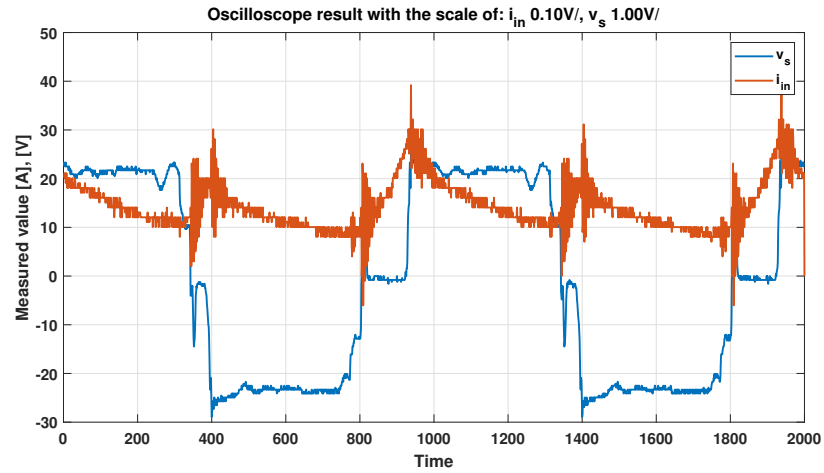
Figure 4.6: Input boost current and secondary side transformer voltage with clamp circuit, $V_{in} = 19.95V$, $D = 0.6$.
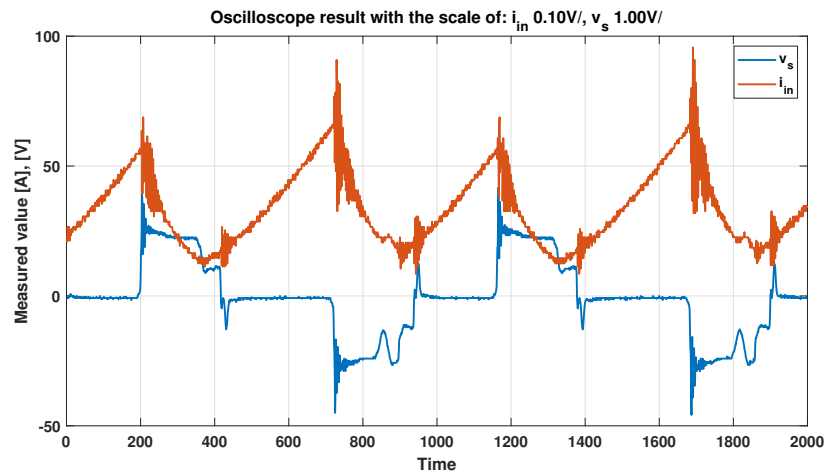
Figure 4.7: Input boost current and secondary side transformer voltage with clamp circuit, $V_{in} = 11.95V$, $D = 0.8$.

Table 4.7: The Output Result of converter without clamp circuit (Frequency = $20k$Hz, Load = 20Ω).

Duty cycle	Input voltage	Input current	Input power	Output voltage	Output power	Efficiency
$Step1, 1, D = 0.6$	$19.95V$	$1.46A$	$29.12W$	$20.25V$	$20.50W$	70.40%
$Step1, 2, D = 0.8$	$9.95V$	$2.65A$	$26.24W$	$15.28V$	$11.67W$	44.50%

Table 4.8: The Output Result of converter with clamp circuit (Frequency=$20k$Hz, Load = 20Ω).

Duty cycle	Input voltage	Input current	Input power	Output voltage	Output power	Efficiency
$Step2, 1, D = 0.6$	$19.95V$	$1.47A$	$29.32W$	$20.39V$	$20.71W$	70.63%
$Step2, 2, D = 0.8$	$9.90V$	$2.58A$	$25.54W$	$15.25V$	$11.63W$	45.54%
$Step2, 2, D = 0.8$	$11.95V$	$3.49A$	$41.71W$	$19.62V$	$19.25W$	46.15%
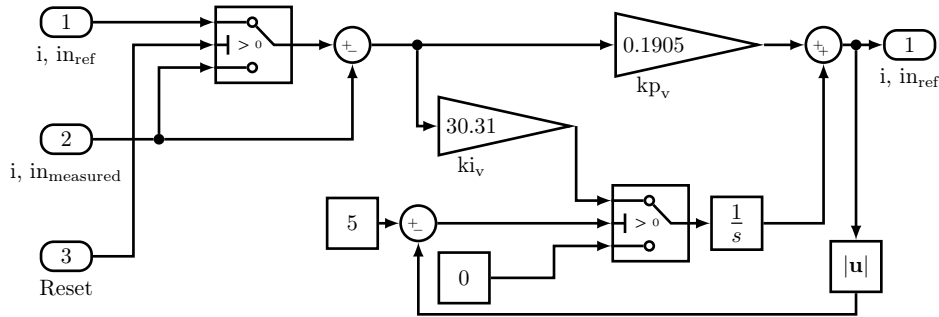
Figure 4.8: The outer PI controller with input reset and anti windup.
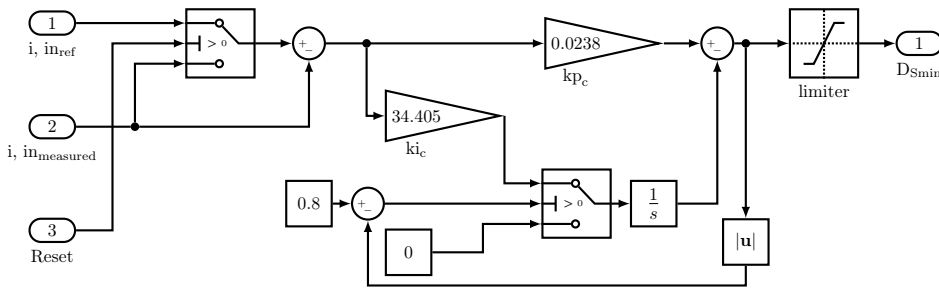
Figure 4.9: Inner PI controller with input reset and anti windup

to the dSPACE through the pin $Al1ch1$. The designed control algorithm in Simulink is shown in appendix G. Using dSPACE, the control algorithm can be built in Simulink, before it is compiled to a real-time program that can control actual hardware. The ControlDesk software is used to interface the host PC to dSPACE platform. This software allows the user to build user interfaces that can give input to the system, while also recording and displaying data in real-time.

Two tests are applied to check the operation of the controller. In the first test, the input voltage is kept fixed and output voltage tracking is checked while the reference voltage is changing. Figure 4.10 shows the variation of output voltage as the reference voltage changes while keeping the input voltage constant (the data are collected from ControlDesk software and plotted in MATLAB). Input boost inductance current ($i_{in,measured}$) and the duty cycle of main switches (Duty cycle) are also shown in the same plot. As it is expected, the duty cycle is increasing while the reference voltage rises and makes the output voltage follows the reference.

The output voltage is supposed to reach $V_o = 20V$ when $V_{in} = 12V$ and $D_{max} = 0.8$, but it cannot go higher than $18.5V$ due to limitations of the duty cycle. The losses from the additional sensors, like all other non-ideal elements, result in increasing the power losses and reducing the efficiency. Then, switches are needed to be in on-state for a longer time to provide the desired constant

output voltage. The duty cycle of main switches is upper bounded by 0.8, because the whole system is designed based on the $D_{max} = 0.8$, At the duty cycle above this value, the amount of current drawn from power supplies exceeds expected. Moreover, the accuracy of the measuring devices is also an issue that can have an effect on the system.

As shown in Figure 4.10, the output voltage stays in steady as the duty cycle varies from 0.5 to 0.8.

For the second test, the reference voltage is kept constant at $20V$ and the
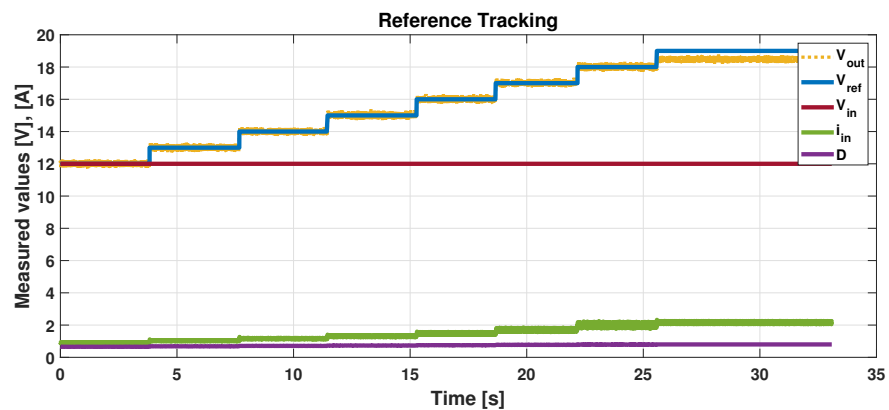
Figure 4.10: Reference tracking test, varied reference voltage and fixed input voltage $V_{in} = 12V$.
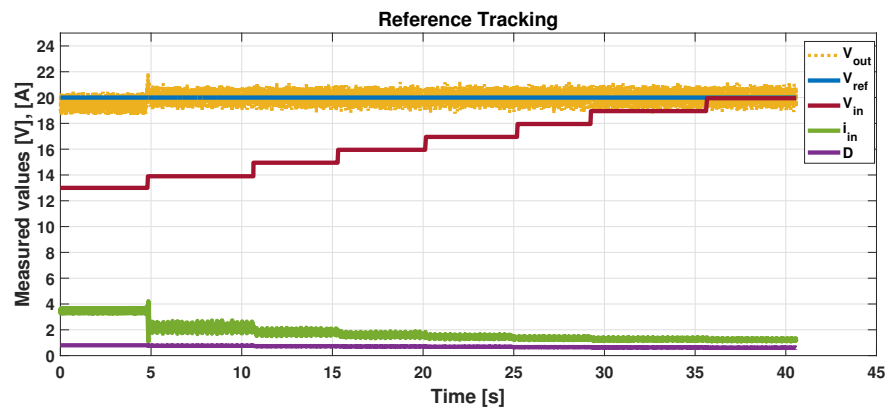
Figure 4.11: Reference tracking test, varied input voltage and fixed reference voltage $V_{ref} = 20V$.

output voltage is measured as the input voltage increases. The results are shown in Figure 4.11, as the input voltage increases, the input current drops, and the duty cycle of main switches decreases to keep the output voltage constant around the reference voltage. These tests confirm the correctness of the controller operation and tracking reference. Figure 4.12.a shows the

oscilloscope waveforms of the circuit when the reference is set to be $20V$ and the input voltage is the minimum value ($12V$). In this case duty cycle of main switches are maximum of 0.8. And the waveforms in maximum input voltage of $20V$ and duty cycle of 0.62 are shown in Figure 4.12. Besides, the built physical model picture can be found in Figure 4.13

(a)   (b)
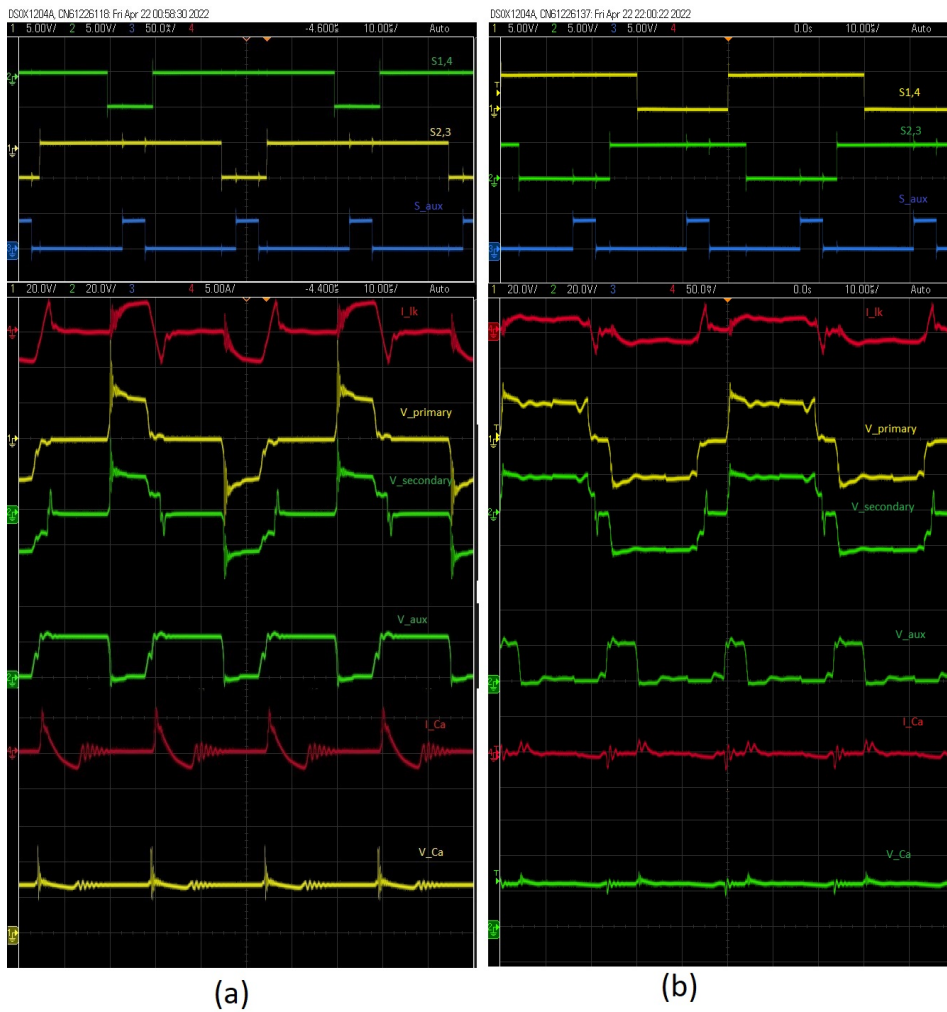
Figure 4.12: The waveforms of the circuit in (a) Minimum input $V_{in} = 12V$, $D = 0.8$ (b) Maximum input $V_{in} = 20V$, $D = 0.62$.
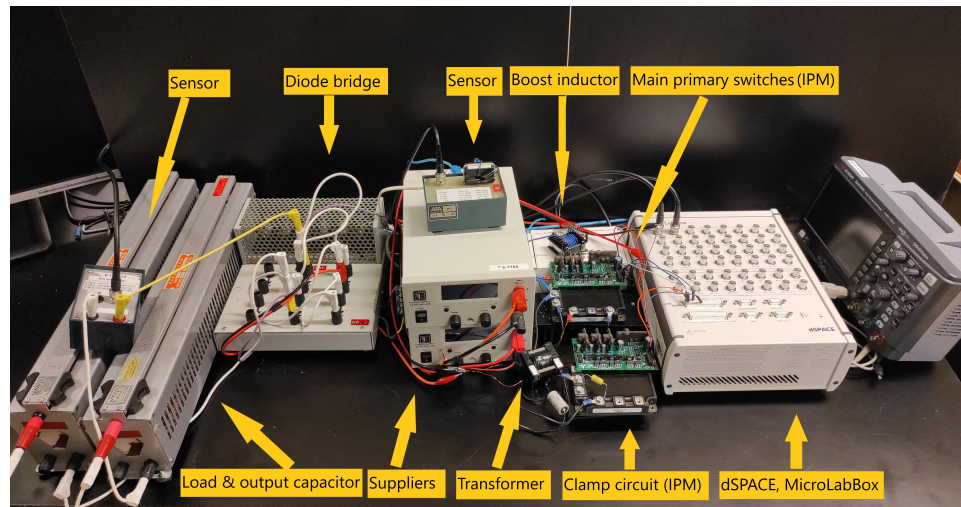
Figure 4.13: The experimental model in the laboratory.

4.3   Analysis of Losses and Efficiency

As can be seen in Table 4.8, the performance of the system even with the presence of the clamp circuit is not satisfying. Based on the observation by a thermometer, the temperature of the main switches (the IPM) and transformer are so high while working. In order to improve the efficiency of the circuit, first, the losses and their causes are needed to be investigated.

4.3.1   The Effect of Input Voltage, Frequency, and Load

The circuit without a controller is tested in higher and lower frequencies with the varied input voltage to clarify the effect of frequency on the efficiency of the system. The results are shown in Table 4.9 and Table 4.10 (Both experiments are done in the duty cycle of 0.6 (as the maximum input voltage) and 0.8 (as the minimum input voltage)). These two tables are simplified in Figure 4.14. As can be seen, the performance of the circuit increases while the input voltage goes higher and the working frequency decreases.

  The impact module used in the experiment is designed for power switching applications operating at frequencies from $5k$Hz to $20k$Hz, $1200V$, and $50A$. The working counditions in this experiment is far lower than the voltage and current range of the module.

The one reason for better efficiency in higher voltage operation condistion might be the voltage drops across the IPM elements are almost constant regardless of the voltage operation range. On the other word, the voltage drops across the emitter-collector of IGBTs and diodes in IPM are significant relative to the input voltage $12 - 20V$ of the circuit and cannot be ignored. In higher voltage

Table 4.9: Efficiency of Circuit vs Varied Input Voltage and Frequency ($D = 0.6$).

Load=20Ω, Duty cycle of main switches=0.6								
Frequency	**Parameter**	**Measured values**						
$f_s = 40kHz$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.8A	1.46A	2.09A	2.75A	3.49A	4.24A	4.96A
	V_o	7.36V	14.25V	20.69V	26.99V	33.78V	40.81V	47.50V
	η	33.86%	46.21%	51.08%	52.98%	54.49%	56.11%	56.86%
$f_s = 20kHz$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.63A	1.06A	1.50A	1.96A	2.41A	2.91A	3.36A
	V_o	8.45V	14.3V	20.24V	26.22V	32.38V	38.62V	44.72V
	η	56.67%	64.10%	68.11%	70.01%	72.81%	73.47%	74.40%
$f_s = 10kHz$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.58A	0.98A	1.39A	1.83A	2.25A	2.74A	3.17A
	V_o	8.62V	14.47V	20.38V	26.39V	32.25V	38.67V	44.81V
	η	64.06%	70.98%	74.70%	75.96%	77.04%	77.96%	79.17%

Table 4.10: Efficiency of Circuit vs Varied Input Voltage and Frequency ($D = 0.8$).

Load=20Ω, Duty cycle of main switches=0.8							
Frequency	**Parameter**	**Measured values**					
$f_s = 40kHz$	V_{in}	5.00V	7.00V	10.00V	12.00V	13.90V	15.00V
	I_{in}	0.91A	1.59A	2.60A	3.50A	4.40A	4.89A
	V_o	4.48V	7.69V	12.14V	15.68V	19.40V	21.32V
	η	22.06%	26.57%	28.34%	29.27%	30.66%	30.98%
$f_s = 20kHz$	V_{in}	5.00V	7.00V	10.00V	12.00V	13.90V	15.00V
	I_{in}	0.91A	1.54A	2.60A	3.34A	4.06A	4.49A
	V_o	5.46V	9.27V	15.16V	19.31V	23.37V	25.65V
	η	32.76%	39.86%	44.20%	46.52%	48.39%	48.84%
$f_s = 10kHz$	V_{in}	5.00V	7.00V	10.00V	12.00V	13.90V	15.00V
	I_{in}	0.84A	1.45A	2.51A	3.26A	3.97A	4.37A
	V_o	5.82V	9.87V	16.12V	20.45V	24.71V	26.95V
	η	40.32%	47.99%	51.76%	53.45%	55.12%	55.40%

(a)   **(b)**
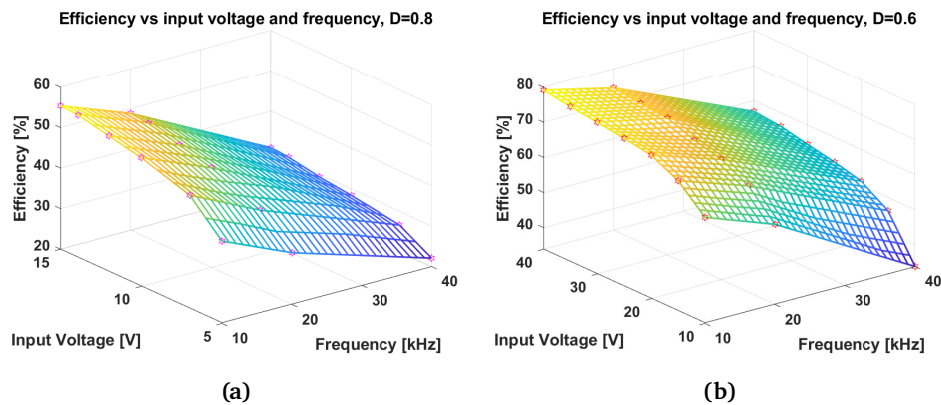
Figure 4.14: Efficiency of circuit vs input voltage and frequency, (a) When $D = 0.8$, (b) When $D = 0.6$.

Table 4.11: Efficiency of Circuit vs Varied Load and Input Voltage ($D = 0.6$).

Frequency=$20k$Hz, Duty cycle of main switches=0.6							
Load	**Parameter**	**Measured values**					
$R_L = 10\Omega$	V_{in}	10.00V	15.05V	20.05V	25.05V	29.20V	$--$	$--$
	I_{in}	1.14A	1.95A	2.79A	3.65A	4.38A	$--$	$--$
	V_o	7.77V	13.23V	18.79V	24.43V	29.23V	$--$	$--$
	η	52.96%	59.64%	63.12%	65.27%	66.80%	$--$	$--$
$R_L = 20\Omega$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.66A	1.10A	1.55A	2.02A	2.47A	2.96A	3.45A
	V_o	8.58V	14.40V	20.33V	26.37V	32.54V	38.71V	44.89V
	η	55.77%	62.63%	66.50%	68.71%	71.45%	72.32%	73.01%
$R_L = 30\Omega$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.47A	0.78A	1.09A	1.41A	1.71A	2.04A	2.37A
	V_o	9.04V	15.01V	21.06V	27.19V	33.46V	39.77V	46.09V
	η	57.96%	63.97%	67.65%	69.77%	72.75%	73.75%	74.69%
$R_L = 40\Omega$	V_{in}	10.00V	15.05V	20.05V	25.05V	30.00V	35.00V	40.00V
	I_{in}	0.37A	0.61A	0.84A	1.07A	1.31A	1.57A	1.82A
	V_o	9.37V	15.47V	21.59V	27.79V	34.1V	40.44V	46.95V
	η	59.32%	65.17%	69.19%	72.03%	73.97%	74.40%	75.70%

operation conditions, this constant drops have a lower effect on the efficiency of the system.

The switching frequency $20k$Hz is another assumption taken at the starting point. When switching frequency decreases, the effect of parasitic elements in the circuit is reduced. Then, the losses in switches drops and surely cause an increment in the efficiency.

Load is another influential factor in the system's efficiency. By increasing the load, the current passing through the circuit reduces, and as a result, efficiency increases. Several tests have been done on the circuit withe varied input voltage and load. Table 4.11 and Table 4.12 show the result of change in load and input voltage on the efficiency. As expected, performance of circuit improves with higher load and input voltage.

4.3.2   Zero Voltage Switching

Ideally, with the active clamp circuit, the leakage energy is not dissipated but can instead be used for Zero Voltage Switching (ZVS) of the bridge switches [29]. From the simulation waveforms in Section 3.4, it was seen that soft-switching is obtained for all the switches. The switches were turned on only when the voltage across them are zero (ZVS).

In the experimental model, the gate-source and drain-source voltages of one of the main switches are shown in Figure 4.16 (The data are collected from an oscilloscope and plotted in MATLAB). The off and on-states in Figure 4.16b and Figure 4.16c show the system is far from soft-switching. The clamp circuit which was supposed to improve the performance of the circuit with ZVS is not

Table 4.12: Efficiency of Circuit vs Varied Load and Input Voltage ($D = 0.8$).

Frequency=$20k$Hz, Duty cycle of main switches=0.8							
Load	**Parameter**	**Measured values**					
	V_{in}	5.00V	7.00V	10.00V	10.80V	$--$	$--$	$--$
$R_L = 10\Omega$	I_{in}	1.36A	2.39A	3.95A	4.38A	$--$	$--$	$--$
	V_o	4.35V	7.53V	12.33V	13.62V	$--$	$--$	$--$
	η	27.83%	33.89%	38.49%	39.22%	$--$	$--$	$--$
	V_{in}	5.00V	7.00V	10.00V	12.00V	13.90V	15.00V	$--$
$R_L = 20\Omega$	I_{in}	0.92A	1.59A	2.60A	3.50A	4.40A	4.89A	$--$
	V_o	5.51V	9.38V	15.30V	19.41V	23.42V	25.20V	$--$
	η	33.00%	39.78%	44.50%	46.44%	48.12%	48.65%	$--$
	V_{in}	5.00V	7.00V	10.00V	12.00V	13.95V	15.05V	17.80V
$R_L = 30\Omega$	I_{in}	0.73A	1.21A	2.01A	2.60A	3.19A	3.49A	4.38A
	V_o	5.95V	10.07V	16.44V	21.00V	25.41V	27.77V	33.94V
	η	32.33%	39.91%	44.82%	47.12%	48.36%	48.94%	49.25%
	V_{in}	5.00V	7.00V	10.00V	12.00V	13.95V	15.05V	17.95V
$R_L = 40\Omega$	I_{in}	0.58A	0.96A	1.56A	2.01A	2.48A	2.75A	3.47A
	V_o	6.17V	10.36V	16.73V	21.40V	26.01V	28.73V	35.74V
	η	32.82%	39.93%	44.85%	47.47%	48.89%	49.86%	51.27%

(a)

(b)
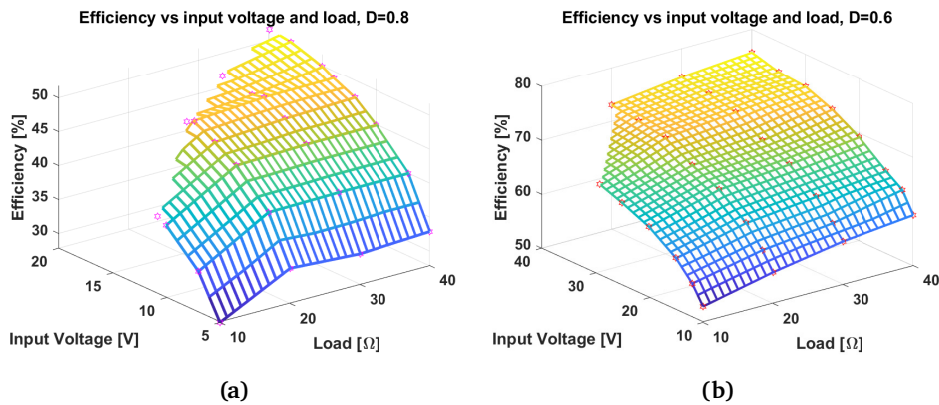
Figure 4.15: Efficiency of circuit vs input voltage and load, (a) When $D = 0.8$, (b) When $D = 0.6$.

working properly. The gate signal and voltage across the auxiliary switch are also shown in Figure 4.17. The power losses due to hard-switching are one of the reasons for the low efficiency of the system.

(a)

(b)

(c)
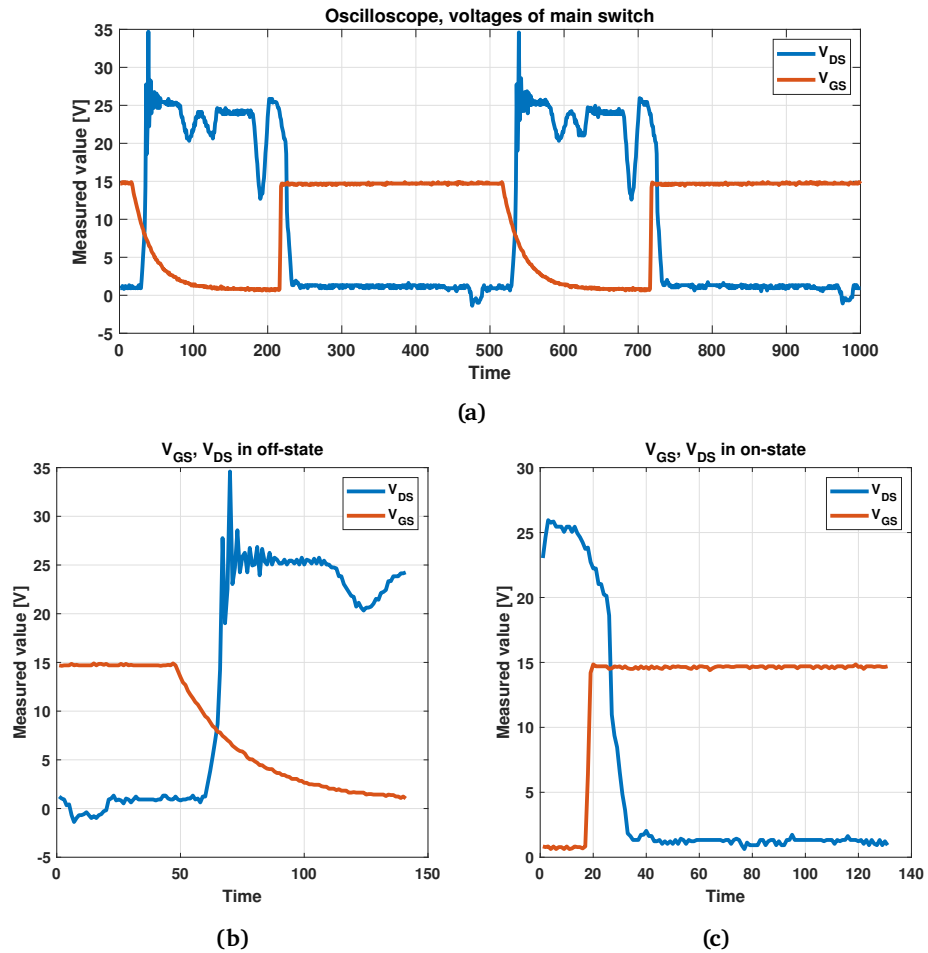
Figure 4.16: (a) Gate-source, drain-source voltages across the main switch, $V_{in} = 1000V$ and $D = 0.62$, (b) Off-state (c) in On-state.

4.3.3   Fast Fourier Transform

The Fast Fourier Transform (FFT) analysis of leakage current waveform captured by the oscilloscope is shown in Figure 4.18. A comparison of these figures with the results in Section 3.5 depicts more harmonic distortion in the real-time model.

Among all frequency components, the largest amplitude of around 24.6dB belongs to the first harmonic which is the switching frequency of the system
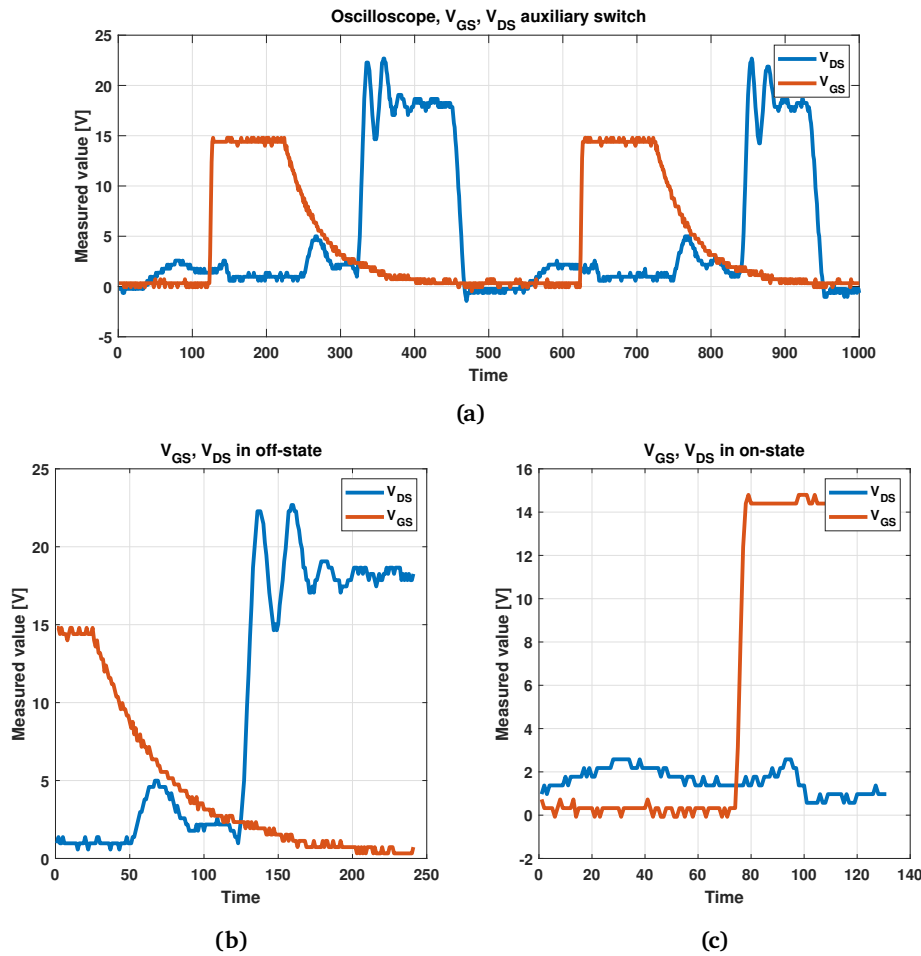
Figure 4.17: (a) Gate-source, drain-source voltages across the auxiliary switch, (b) Off-state (c) On-state.

$20k$Hz. However, the amplitude of the third, sixth, and some other harmonics are quite high and it shows that there are some noise sources in the system. Harmonics in transformers cause an increase in the iron losses in the magnetic core, as well as copper losses. Voltage distortion increase losses due to hysteresis and eddy currents and causes overstressing of the insulation material used. Besides, the increase in transformer eddy current loss due to harmonics has a significant effect on the operating temperature of the transformer.

These harmonics are might caused due to long connecting wires, the distance between elements and the common ground, etc. Apart from the IPMs, diode bridge, and load, the rest of the system can be built on the Printed Circuit Board (PCB). This may reduce the harmonics while decreasing wiring in the circuit. Moreover, it may be very helpful to design harmonic filters to suppress harmonic propagation [43].
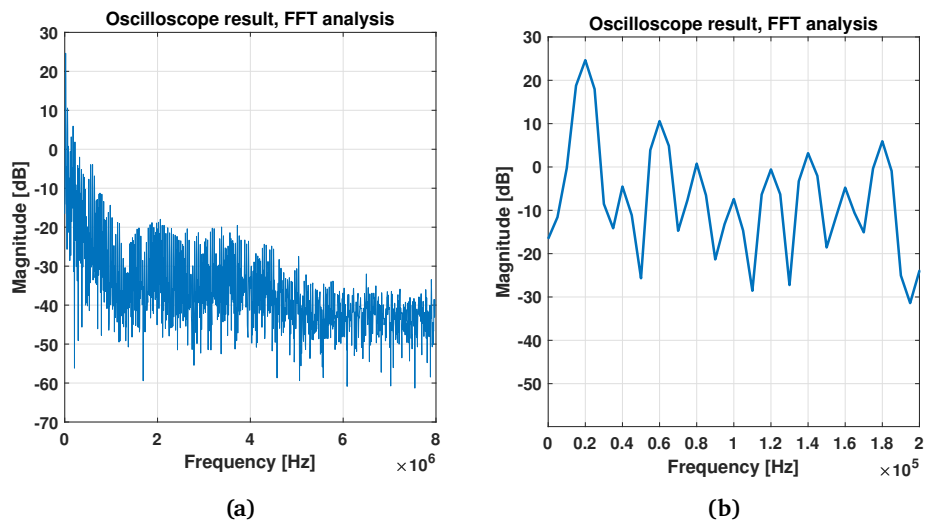
Figure 4.18: (a) FFT analysis of the physical model, (b) The closer look at harmonics.

/5

Discussion and future work

The efficiency of the designed circuit is about 97% in simulation while efficiency in the laboratory, in minimum voltage of FC, is less than 50% and in maximum voltage is around 70%. The circuit is tested under different input voltages, frequencies, and loads in order to realize the causes of this relatively poor performance. It is observed that the performance of the system is improved with higher voltage, lower frequency, and higher loads.

Better efficiency in higher voltage might be due to constant voltage drops across switches in IPM. It means in a low input voltage situation, the switching losses are quite considerable compared to the total power transferred through the system and have a severe effect on the performance of the converter.

In lower frequencies, the number of off and on-states of the switches decreases which results in lower switching losses. Moreover, parasitic capacitance present in a circuit is unlikely to cause any major issues for low-frequency designs. As the frequency increases, these unwanted capacitances act as a short circuit and cause more leakage current and eventually more power losses and lower efficiency. Besides, the increment of core losses in higher frequencies cannot be ignored.

Increasing the load also improves the performance of the circuit. As load increases, the current flowing through the circuit decreases thus the conduction losses, which are proportional to the square of the current, are also cut down resulting in an improvement in the efficiency.

Zero Voltage Switching (ZVS) explained in theory, is investigated in simulation on MATLAB. The main switches are gated for ZVS turn-on and off, however, the turn-off loss in the clamp switch is noticeable. As the switching frequency

of the auxiliary circuit is twice of that the main switches, this turn-off loss contributes a significant portion to the total power loss of the system. Using the different methods in designing clamp capacitors may reduce the turn-off losses.

Comparing simulation results with the laboratory confirms more losses in the physical model. Apart from losses in auxiliary switch, main switches do not gate for ZVS turn on which explains the low efficiency of the system partially. The reason might be the snubber capacitances of the switches are not discharging completely by the leakage inductance current before the on-gate signal. In order to minimize losses, a soft-switching active clamp scheme utilizing the resonance between the clamp capacitor and the leakage inductor is proposed in [32].

Also, it is noticeable that the design method was based on the MOSFET but in the physical model, IGBTs are used as the switches. It means in order to gate Zero Current Switching (ZCS) for IGBTs, there is a need for a more precise design of the time delay between the auxiliary switch and main switches.

The differences between the Fast Fourier Transform (FFT) analysis of simulation and the physical model show the harmonic noises in the built model. These noises are mainly caused due to the distance of elements from the common ground, long wiring in the circuit, poor connection between elements, etc. Harmonics in the transformer increases the core and copper loss and hence reduces its efficiency. Other problems include possible overheating of neutral wires, transformer heating, malfunctioning of power factor correction capacitors, power generation and transmission losses, and finally the poor performance of the system.

Last but not least, as the physical model suffers from hard-switching, the design method for the auxiliary clamp circuit or even the converter type are needed to be revised. The resonance converters might be a good solution for this problem. The resonant version of the full-bridge current-fed converter with ZCS is proposed in [24]. Based on the proposed method, the current-fed full-bridge converter utilizes the leakage inductance and parasitic capacitance of the high-voltage transformer to achieve ZCS operation, thus allowing reductions in voltage and current spikes on the power devices, as well as decreasing the switching losses of the converter [24].

As the resonant tank decreases overshoots of voltages over switches, there is no longer a need for an additional clamp circuit, which means no auxiliary switch losses and better efficiency. Another benefit of this converter is that the rectifier diodes on the high-voltage (or secondary)side are operated with ZCS. Therefore, the rectifier diodes do not suffer from reverse-recovery problems and better efficiency can be reached.

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Conclusion

This thesis investigates one of the most favorable converters for integrating fuel cells into a DC microgrid. A current-fed full-bridge isolated DC-DC converter has advantages such as high voltage conversion ratio, low switches' losses, and low input current ripple which make it one of the best choices for Fuel Cells (FC). The transformer in the converter can solve the lack of galvanic isolation in FC to some extent by creating a barrier between the FC and loads. Active-clamp snubs the voltage turn-off spike and aids in Zero Voltage Switching (ZVS) of the switches. This converter transfer power to the load through the leakage inductance which can be controlled by regulating the duty cycle of switches in order to have the constant DC voltage link regardless of the changes in the output of the FC stack.

The simulation of the designed circuit is done in MATLAB and Simscape for high voltage and the efficiency of the system is measured in the ideal situation which is around 97%. In order to verify the theory of design procedure and the simulations, the whole system is redesigned with scaled values for implementing the circuit in the laboratory.

Two Intelligent Power Modules (IPM), designed transformer, diode bridge, and other complementary components are used for the converter in the laboratory. The Simulink of the control algorithm is done in MATLAB which is connected to the dSPACE 1202 setup (ControlDesk software and MicroLabBox). The efficiency of the built model varies from 50% in minimum input voltage, and 70% in maximum input voltage case. The zero voltage switching, reached in simulation, does not exist in the physical model. Besides, more harmonic distortion is observed in the experimental model. The performance of the physical model

is analyzed by manipulating some effective factors in the system and it can be seen that the efficiency of the system gets better in higher voltage range, higher load, and lower frequency conditions.

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/A

Simulation of current-fed full-bridge isolated DC-DC converter with clamp circuit in MATLAB.

The simulation of current-fed full-bridge isloated converter with a clamp circuit

Main switch pulse 20kHz   S 14   S 14   [S14]

0.5   /20000   S 23   [S23]
phase shift

Auxiliary switch pulse 40kHz   G aux   [Gaux]
G, aux

1.63   /40000   phase shift1

Discrete
1e-07 s.

[S14]   [S23]

L =8mH

Caux

[S23]   [S14]

[Gaux]

Vin

Ca=4.56uF

L_lk=9.04 uH

1   2   Lm=0.18mH

Co=3.2mF   RL=2.5

n=1

/B
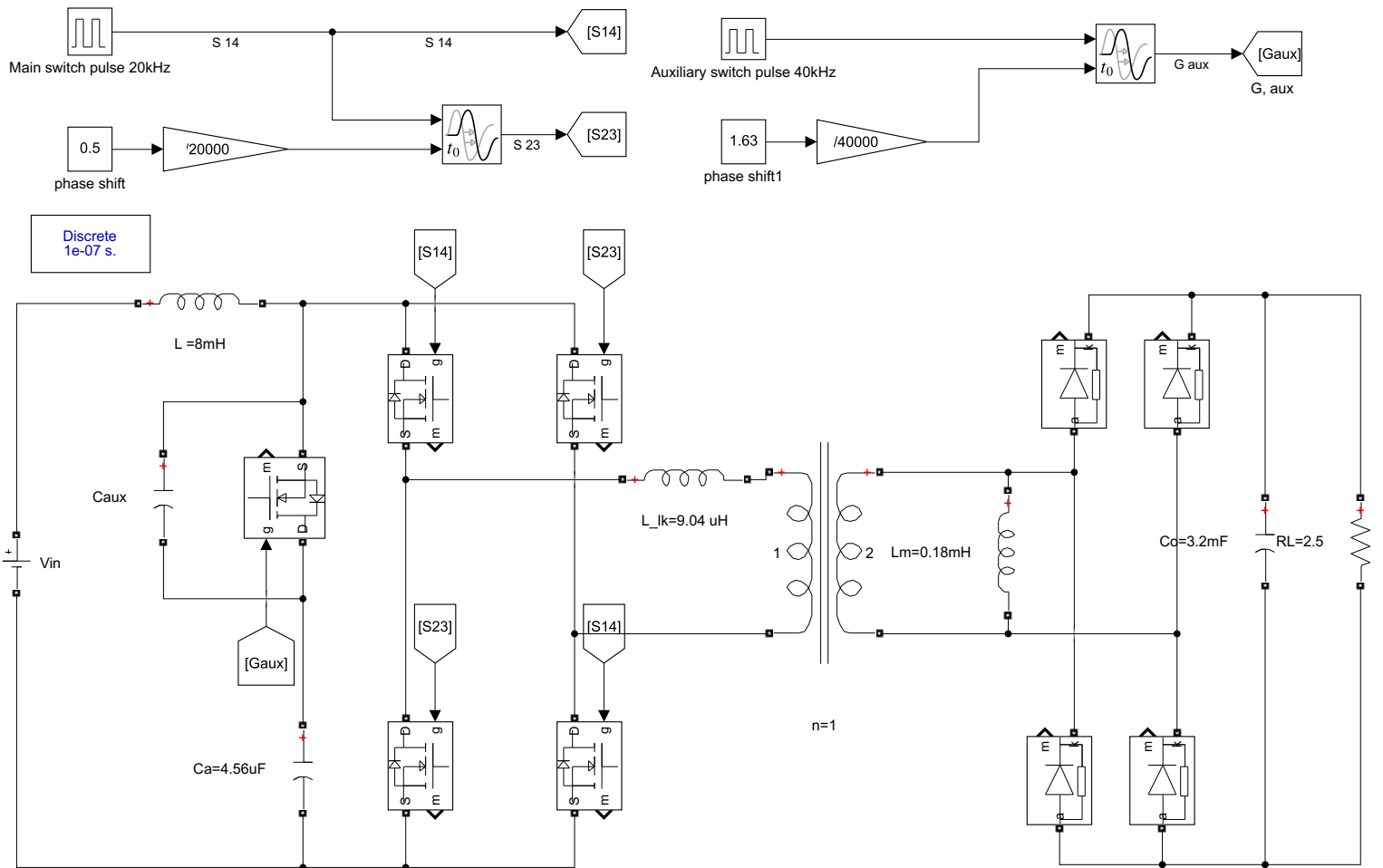
Simulation of the current-fed full-bridge isolated DC-DC converter with clamp circuit and controller in MATLAB.

The simulation of current-fed full-bridge isloated converter with a clamp circuit and controller

/C
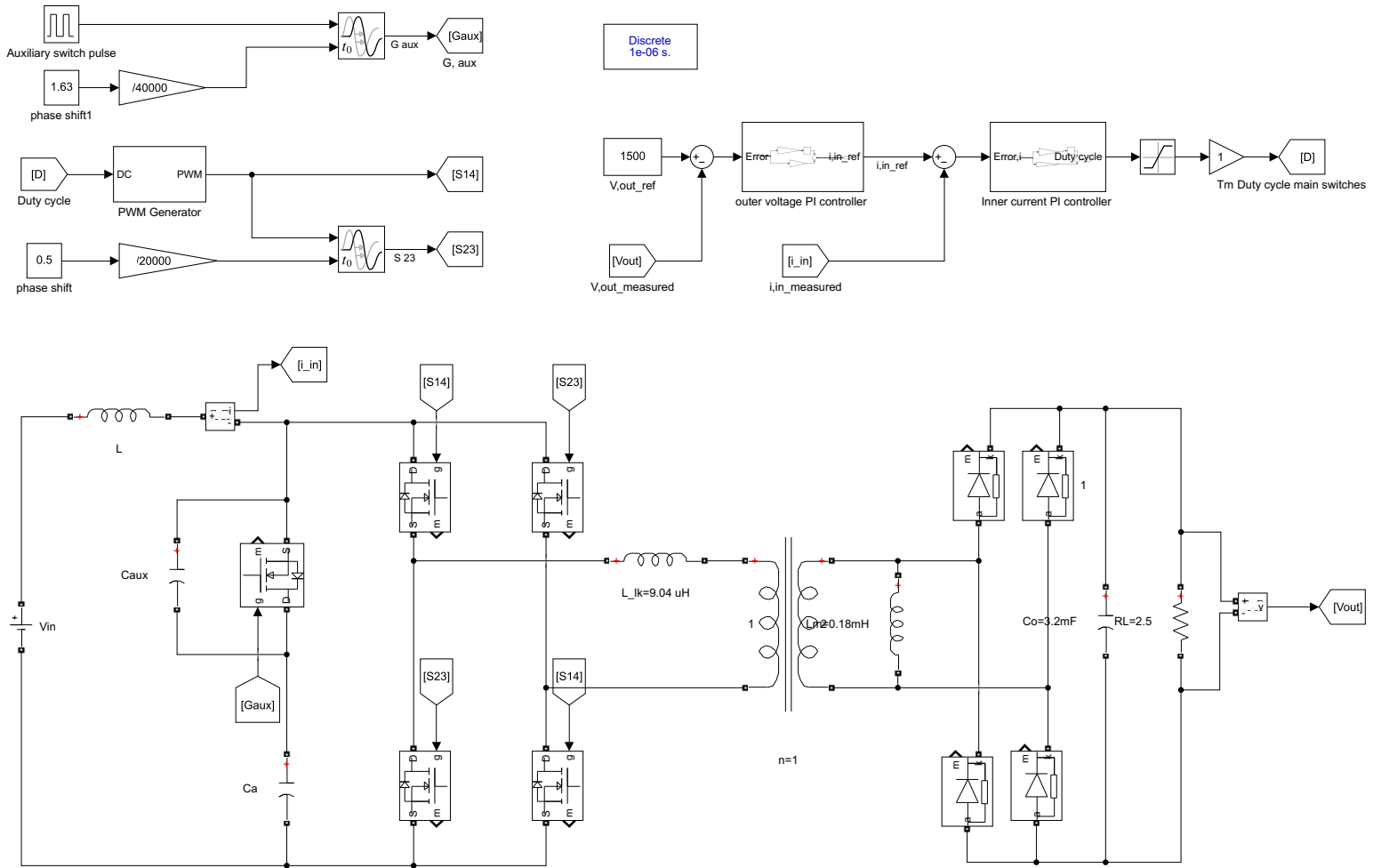
Simulation of the current-fed full-bridge isolated DC-DC converter with clamp circuit and controller in Simscape.

The simulation of current-fed full-bridge isloated converter with a clamp circuit and controller (Simscape)
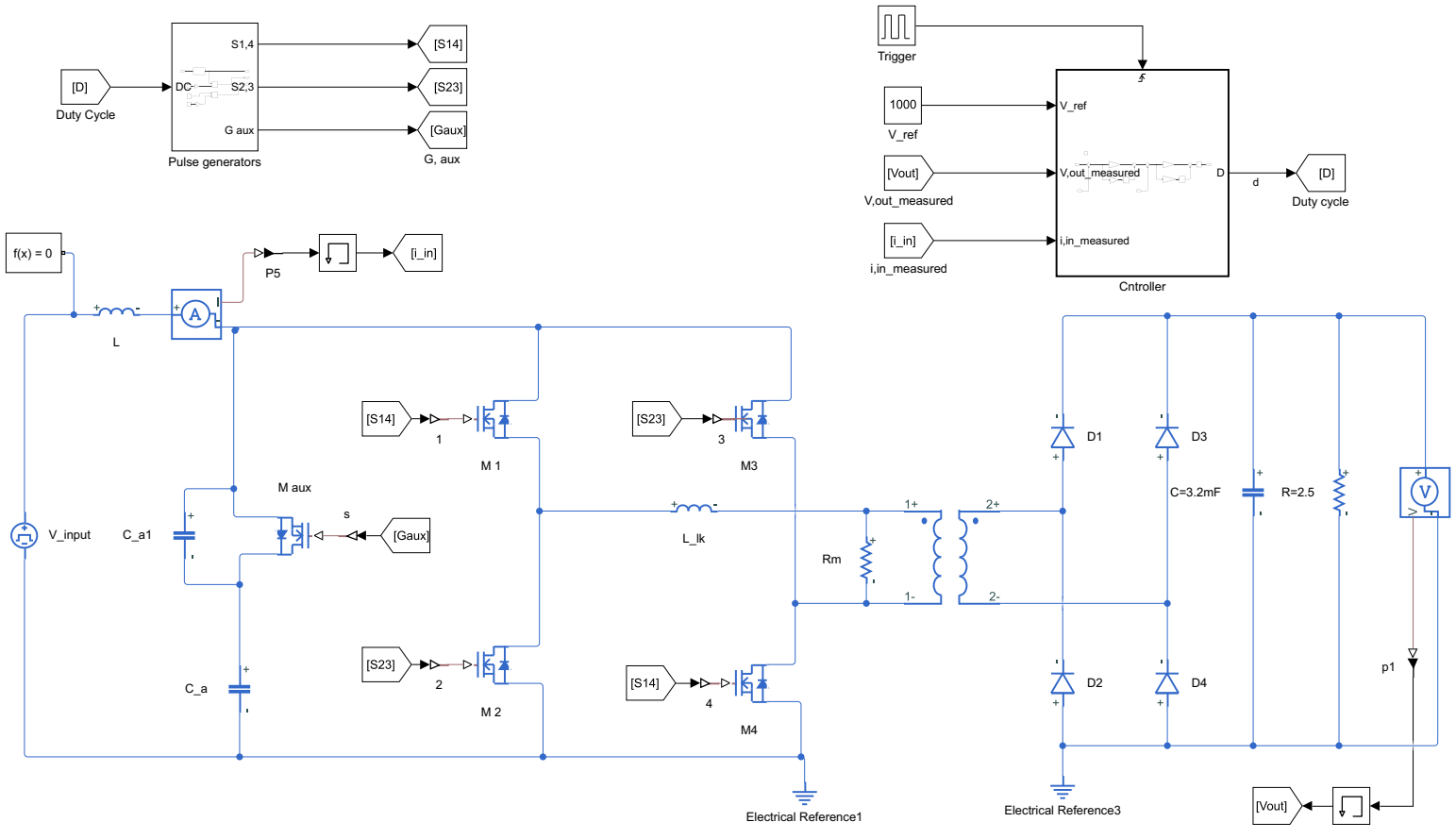
The simulation of controller subsystem (Simscape)

/D
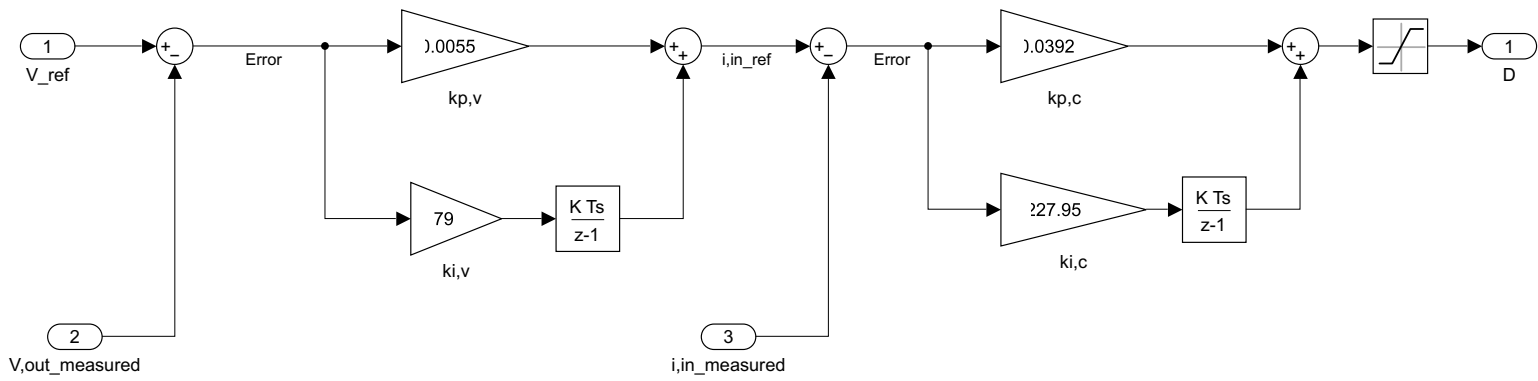
MATLAB codes for designing and calculating the physical model converter, transformer, and controllers.

1. Designing the current-fed full-bridge converter with a clamp circuit

```matlab
% assumption:
V_in_min= 12;          %minimum input voltage
V_in_max=20;           % maximum input voltage
V_o= 20;               % output voltage (I_out=4)
P_o= 20;               % output power
P_o_min=2;             % minimum load 10%
f_s= 20e3;             % switching frequency
f_clamp=2*f_s;         % clamping frequency twice as switching frequency
effi_assume= 1;        % assuming efficiency is 100%
D_max=0.8;             % maximum duty cycle
R_L = ((V_o^2)/P_o)

% Average input current
I_in_av= (P_o)/(effi_assume*V_in_min)

% maximum switch voltage rating
V_sw_max= (V_in_min)/(2*(1-D_max))
% ----------------------------------------------------------------

%Leakage inductance performing in minimum input voltage and full load
% L_rate=L'_m / L_lk parallel inductance in primary side over leakage
inductance
% n is tranformer turn ratio secondary to primary side
for n=0.5:0.1:1
    L_rate=10:50;
    L_lk= (R_L./f_s).*(((((V_in_min./V_o).^2)./(4.*(1+(1./L_rate))))-
(((V_in_min./V_o).*(1-D_max))./(2*n)));
    hold on
    grid on
    figure(1);
    plot(L_rate,L_lk)
    xlabel('L_m/L_lk')
    ylabel('L_lk')
end
hold off
% ----------------------------------------------------------------

% the leakge inductance must be the value that D>0.5 ,
% Smaller value of L_p_m/Llk will achieve ZVS at light load but
increase peak and rms currents through
% the switches, leading to low efficiency of the converter
% Also increased number ot turn ratio result in higher conduction loss
and low effcuency.
% thus we need, low L_p_m/Llk  ratio, and low RMS current over switches
and
```

```matlab
% low transformer turn ratio.

for n=0.6:0.1:1
    L_rate=10:50;
    % Conduction time of rectifier diodes:
    T_DR=(n.*V_in_min)./(2.*V_o.*f_s.*(1+(1./L_rate)));
    % Leakage inductance wee need in primary side
    L_lk= (R_L./f_s).*(((((V_in_min./V_o).^2)./(4.*(1+(1./L_rate))))-
(((V_in_min./V_o).*(1-D_max))./(2*n)));
    % Magnetizing inductance in seconday side
    L_m=L_lk.*L_rate.*(n.^2);
    % duty cycle based on the leakage and magnetizing inductance and
load
    D=1-
(((((2.*n.*V_o)./V_in_min).*(((V_in_min./V_o).^2)./(4.*(1+(1./L_rate)))-
((L_lk.*f_s)./R_L))));
    % the peak value of magnetizing current reflected to the primary
side
    I_Lm_p_peak=(n.*V_o.*T_DR)./(2.*L_m);
    % RMS current over swtiches
    I_sw_rms=sqrt(((I_in_av.^2).*(0.75-
(D/2)+((T_DR.*f_s)./3)))+((I_Lm_p_peak.^2).*((2./3)+(D./3)-
((4.*T_DR.*f_s)./3)))+(I_in_av.*I_Lm_p_peak.*(D-1+((T_DR.*f_s)./3))));
    hold on
    grid on
    figure(2);
    plot(L_rate,I_sw_rms)
    xlabel('L_m/L_lk')
    ylabel('I_sw_rms')
    end
hold off
% -----------------------------------------------------------------

% assumption based on the above calcullation
D=0.6;
n=1;                % transformer ratio
D_max=0.8;          % maximum duty cycle
dI_in=0.1;          % boost inductor ripple current
L_rate=30;          % inductance ratio L_p_m/Llk
dV_ca=1;            % ripple voltageof auxiliary capacitpr
dv_o=0.01;          % Allowable ripple in output voltage.

% leakage inductance
L_lk= (R_L./f_s)*(((((V_in_min/V_o)^2)/(4*(1+(1/L_rate)))))-
(((V_in_min/V_o)*(1-D_max))/(2*n)));

% magnetizing inductance
```

```matlab
L_m=L_lk*L_rate*(n^2);
% -----------------------------------------------------------------

% assumption for switches
t_f=70e-9;
C_oss=1.54e-9;
L_lk=12e-6
L_m=1.45e-3

% maximum voltage across the inductor =Vca
V_ca=(V_in_min)/(2*(1-D_max));

% input boost inductor
L=(V_in_min*(D-0.5))/(dI_in*f_s)

% Conduction time of rectifier diodes:
T_DR=(n*V_in_min)./(2*V_o*f_s*(1+(1/L_rate)))

% the peak value of magnetizing current reflected to the primary side
I_Lm_p_peak=(n*V_o*T_DR)/(2*L_m)

% The RMS current through leakage inductance
I_Llk_rms=sqrt(((I_in_av^2)*((8*T_DR*f_s)/3))+((I_Lm_p_peak^2)*((4*D/3)
-1/3))+((I_in_av*I_Lm_p_peak)*((8*(D-1)/3)+4*T_DR*f_s)));

% peak current through leakage inductance
I_Llk_p_peak= 2*I_in_av +I_Lm_p_peak

% maximum current across leakage inductance
V_Llk_p_max= V_o/n

% The RMS current through magnetizing inductance
I_Lm_rms=(I_Lm_p_peak/n)* sqrt(1-((8*T_DR*f_s)/3))

% peak magnetizing inductance current
I_Lm_peak=I_Lm_p_peak/n

% maximum current across magnetizing inductance
V_Lm_max= V_o

% RMS current over swtiches
I_sw_rms=sqrt(((I_in_av^2)*(0.75-
(D/2)+((T_DR*f_s)/3)))+((I_Lm_p_peak^2)*((2/3)+(D/3)-
((4*T_DR*f_s)/3)))+(I_in_av*I_Lm_p_peak*(D-1+((T_DR*f_s)/3))))

%Peak currents through main switches
I_sw_peak= 2*I_in_av+I_Lm_p_peak
```

```matlab
%average currents through main switches
I_sw_av= I_in_av/2

%RMS current through the auxiliary switch
I_axsw_rms=(I_in_av+I_Lm_p_peak)*(sqrt(2*(1-D)/3))

%peak current through the auxiliary switch
I_axsw_peak= I_in_av+I_Lm_p_peak

% Average current through auxiliary switch
I_axsw_av= (I_in_av+I_Lm_p_peak)*(1-D)/4
% ----------------------------------------------------------------------

%% Auxiliary circuit

% maximum voltage across Auxiliary capacitor
V_ca= (V_in_min)/(2*(1-D_max))

% peak current through Ca
I_ca_peak=I_in_av+I_Lm_p_peak

% Auxiliary clamp capacitor
C_a= ((I_ca_peak/(4*pi*f_s*dV_ca))*sqrt(2*(1-D)/3))

%RMS current through auxiliary capacitor
I_ca_rms = I_ca_peak*sqrt(2*(1-D)/3)

% Average rectifier diode current
I_DR_av= P_o/(2*V_o)

%Voltage rating of rectifier diodes
V_DR=V_o

% Value of output filter capacitor
I_o=P_o/V_o;
C_o=(I_o*((1/(2*f_s))-T_DR))/dv_o

% calculation of snubber capacitors
C_1= ((t_f*(I_in_av+I_Lm_p_peak)*2*(1-D))/(V_in_min))-2*C_oss
C_sax=C_1;

% ----------------------------------------------------------------------
```

2. Designing the transformer

```matlab
%% Transformer design, based on the AP method
% Reference:High-frequency magnetic components by Kazimierczuk, Marian
K

V_in_min=12;                    % minimum input voltage
V_in_max=20;                    % maximum input voltage
V_out=20;                       % output voltage
P_out=20;                       % output power
I_in=P_out/V_in_min;            % input current
f_s= 20e3;                      % frequency
n_effi=0.90;                    % efficiency of converter
D_Bmax=0.8;                     % max duty cycle of converter


% Transfer ratio
n= V_in_min/V_out;
I_out_max = I_in*n;
I_out_min = I_in*n;
M_vdc_min = V_out/V_in_max;
M_vdc_max = V_out/V_in_min;

% output power[W] and load resistance[ohm]
P_out_max= I_out_max*V_out;
R_L_min=V_out/I_out_max;
P_out_min= I_out_min*V_out;
R_L_max=V_out/I_out_min;
n=1;

% magnetizing inductance [H] DCM
L_m =(n^2*R_L_min*(1-D_Bmax)^2)/(2*f_s);

%% Duty cycle in DCM

% max duty cycle at full load    %% just depends on the efficiency and
max duty cycle of converter
D_max = M_vdc_max*(((2*f_s*L_m)/(n_effi*R_L_min))^0.5);

% min duty cycle at full load
D_min = M_vdc_min*(((2*f_s*L_m)/(n_effi*R_L_min))^0.5);

% Max duty cycle when diode is on at full load
D_1max = (((2*f_s*L_m)/((n^2)*R_L_min))^0.5);

check_D= D_max +D_1max;     % less than 1

% max DC input current
```

```matlab
I_in_max = (M_vdc_max* I_out_max)/n_effi;

% maximum current through the primary winding current  and rms value
I_p_max = (D_min* V_in_max)/(f_s*L_m);

I_p_rms_max = I_p_max*((D_max/3)^0.5);

I_p_max=8.6;

% maximum energy stored in the magnetic field of the transformer
W_max = 0.5*L_m*I_p_max^2;

%% asumption for core
K_u = 0.3;        % core window utilization factor
J_m= 5e+6;        % [A/m2] current density
B_pk = 0.32;      % [T]

% the core area product
A_p1 = (4*W_max)/(K_u*J_m*B_pk);   %  minimum value (11.147)

% ------------------------------------------------------------------------

%%  The core details:  3f3 ETD/39/20/13
a=(38.9e-3);
b=(29.3e-3);
c=(12.8e-3);
d=12.8e-3;
h=14.2e-3;

A_c = (125e-6 );              %[m2]  cross section area
W_a= 2*(177e-6);              %[m2] window area (2 ETD)
A_p = 0.5* W_a*A_c ;          %[m4] core area product= window area*core
area
l_c =2*(92.9e-3);            %[m]   lenght
V_c = 11500e-9;              %[m3]  volume
p= 1000                      % resistivity of the ferrite material is
ρc= 1000 cm.
n=1;                         % transformer turn ratio
u_rc= 1650;                  % core permeability
u_0 = pi*4e-7;               % Permeability of free space
B_s = 0.32;                  % saturation flux density for ferritesat
high temperature

% skin path [mm]
sp_w=(66.2e-3)/(f_s^0.5);

% diameter of the bare strand minimum value [mm]
```

```matlab
d_is= 2*sp_w;
% ------------------------------------------------------------------

%% choose the wire from AWG for example AWG 14
d_os= 1.62814e-3 ;                      %[m] inner diameter of wire
d_is= 1.62814e-3;                       %[m] outer diameter of wire
A_wst = 2.08e-6,                        % [m2] conductor cross-section
R_wpDCs_over_l_w =    8.282e-3;         %ohm_per_lenght [ohm/meter]
% ------------------------------------------------------------------

% cross-sectional area of the primary winding wire
A_wp=I_p_max/J_m ;;    %[mm2]

% number of strands in primary winding
S_p= A_wp/A_wst ;

%% pick  number of strands in primary winding (rounded up)
 S_p=1;

% area allocated to the primary winding
W_ap= W_a/2;

% cross-sectional area of the insulated strand wire
A_wp_o = (pi*d_os^2)/4;

%number of turns of the primary winding
N_p_1=(K_u*W_ap)/(S_p*A_wp_o);

N_p=round(N_p_1)

%number of turns of the secondary winding
N_s=N_p/n
% ------------------------------------------------------------------

%% check conditions to check if we work in saturation area or linear
%maximum peak value of the magnetic flux density
l_g =0                                  % air gap
B_pk_c = (u_0*N_p*I_p_max)/(l_g+(l_c/u_rc))   % must be less than B_s

%maximum peak value of the AC component of the magnetic flux density
[T]
B_m=B_pk_c/2
% ------------------------------------------------------------------

%% losses
% the core power loss density  [w/meter] / High frequency magnetic
```

```matlab
% First : Hysteresis losses density

P_h = (4*f_s*u_rc*u_0*(N_p*I_in)^2)/(l_c^2)
P_v = (0.0573*(20^1.66)*((10*B_m)^2.68))*(10e-3)

% core loss [W]
P_c=V_c*P_v

% MTL, the mean turn length
l_T= pi*(c^2);

% length of the primary winding wire
l_wp= N_p*l_T

% ---------------------------------------------------------------------

% DC and low-frequency resistance of each strand of the primary winding
R_wp_DCs= R_wpDCs_over_l_w * l_wp

% DC and low-frequency resistance of the primary winding
R_wp_DC = R_wp_DCs/S_p          %11.165

% DC and low-frequency power loss in the primary winding
P_wp_DC = R_wp_DC*(I_in_max^2);

%%  Harmonic AC resistance factor of primary winding
F_Rph=8.78;

% primary winding loss
P_wp=F_Rph * P_wp_DC;

% maximum current through the secondary winding and rms
I_s_max=I_p_max * n;

I_s_rms_max = I_s_max *((D_1max/3)^0.5);

% cross-sectional area of the total secondary winding wire
A_ws=I_s_max/J_m;

%number of strands of the secondary winding
S_s=A_ws/A_wst;

%length of the secondary winding
l_ws = N_s* l_T;

% DC and low-frequency resistance of each strand of the secondary
winding
```

```matlab
R_ws_DC_s=R_wpDCs_over_l_w*l_ws;

% DC and low-frequency resistance of all strands in the secondary
winding
R_ws_DC = R_ws_DC_s/S_s;

% DC and low-frequency power loss in the secondary winding
P_ws_DC= R_ws_DC* ( I_out_max^2);

%DC and low-frequency power loss in both the windings
P_w_DC= P_ws_DC + P_wp_DC

%% The harmonic AC resistance factor is FRsh= 2.563 for Nls= 1 and
D1max= 0.4734.
F_Rsh= 2.563;

%secondary winding power loss
P_ws= F_Rsh * P_ws_DC;

%power loss of both the windings
P_w=P_ws + P_wp;

% the toal power loss core loss and winding loss
P_cw= P_c + P_w
% ----------------------------------------------------------------------

%% Efficiency

% transormer efficiency
n_t = P_out_max/(P_out_max+ P_cw)
% ----------------------------------------------------------------------
```

3. Finding the transfer functions (Small-signal analysis)

```
% Designing controller for CFC full-bridge with clamp circuit
% for physical model.

% assumptions
V_in_min= 12;          %minimum input voltage
V_in_max=20;           % maximum input voltage
V_o= 20;               % output voltage
V_out_ref= 20;         % reference output voltage
P_o= 20;               % output power
P_o_min=2;             % minimum load 10%
f_s= 20e3;             % switching frequency
f_clamp=2*f_s;         % clamping frequency twice as switching frequency
D_max=0.8;             % maximum duty cycle
R_L=20;
I_L=3.5 ;              % peak value of leakage current
V_ca=30;               % peak value of voltage across the clamp capacitor
Dd=0.02;               % minimum phase shift
n=1;                   %transformer turn ratio
D=0.8;                 % maximum duty cycle of main switches
L=2e-3;                % inout boost inductance
L_lk=12e-6;            %leakage inductance
L_s=L_lk;              %leakage inductance
C_o=1e-3;              % output capacitance

s= tf('s');
A_11=((C_o*C_a)*s^2)+((((1-
D)^2)*C_o/(f_s*L_s))+C_a*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))))*s+((((1-
D)^2)/(f_s*L_s))*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))));
A_12=-(2*(1-D)*C_o)*s-(2*(1-D)*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))));
A_13=-(2*((1-D)^3))/(n*f_s*L_s);
A_21=(2*(1-D)*C_o)*s+(2*(1-D)*((1/R_L)+((2*I_L*(1-
D+Dd))/(n*V_o))))+((2*((1-D)^2)*(1-D+Dd))/((n^2)*f_s*L_s));
A_22=(L*C_o*(s^2))+L*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o)))*s;
A_23=(L*((1-D)^2)*s)/(n*f_s*L_s);
A_31=(((2*C_o*(1-D+Dd))*s)/n)+((2*((1-D)^2)*(1-
D+Dd))/(n*f_s*L_s))+(4*I_L*((1-D)^2))/V_o;
A_32=(((2*I_L*L*(1-D))*s)/V_o)-((4*(1-D)*(1-D+Dd))/n);
A_33=(L*C_a*(s^2))+(((L*((1-D)^2))*s)/(L_s*f_s))+(4*((1-D)^2));
A=[A_11 A_12 A_13; A_21 A_22 A_23; A_31 A_32 A_33];

B=inv(A);

b_1=2*V_ca;
b_2=2*(((1-D)*(V_ca-(V_o/n)))-I_L);
b_3=-(2*I_L*V_ca)/V_o;
```

```matlab
% -------------------------------------------------------------------

%% Transfer function of the system without controller
% Direct TF= vo/D
det_A_v=(1/1)*(((L*C_o*C_a)*(s^3))+((((((1-
D)^2)*C_o*L)/(L_s*f_s))+(L*C_a*((1/R_L)+((2*I_L*(1-
D+Dd))/(n*V_o)))))*(s^2))+(((((L*((1-
D)^2))/(f_s*L_s))*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))))+((4*((1-
D)^2)*C_o)))*s)+(4*((1-D)^2)*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))+(((1-
D)*(1-D+Dd))/((n^2)*f_s*L_s)))));
N_TP_v= (1/1)*[A_31 A_32 A_33]*[b_1; b_2; b_3];

numv=(1/180.8)*[-2.455e08 , 2.33e13 , 4.706e14];
denumv=[1, 6.242e04, 1.917e07, 6.683e08];
TF_D=tf(numv, denumv)

% -------------------------------------------------------------------

%% current controller
% TP1= V_TP_1/ det_A
det_A=(1/3.6e-11)*(((L*C_o*C_a)*(s^3))+((((((1-
D)^2)*C_o*L)/(L_s*f_s))+(L*C_a*((1/R_L)+((2*I_L*(1-
D+Dd))/(n*V_o)))))*(s^2))+(((((L*((1-
D)^2))/(f_s*L_s))*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))))+((4*((1-
D)^2)*C_o)))*s)+(4*((1-D)^2)*((1/R_L)+((2*I_L*(1-D+Dd))/(n*V_o))+(((1-
D)*(1-D+Dd))/((n^2)*f_s*L_s)))));
N_TP_1= (1/3.6e-11)*[A_11 A_12 A_13]*[b_1; b_2; b_3];

% Inner loop TF (current loop)
s=tf('s');
num1=[3e04, 3.149e08, 5.896e10];
denum1=[1, 9386 , 5.62e06 , 1.379e09];
Tp1=tf(num1, denum1)

% -------------------------------------------------------------------

%% Voltage controller
% TP2
Tp_2=((2*(1-D+Dd)))/(((n*C_o*s)+(n/R_L)));

% Outer loop TF (voltage loop)
s=tf('s');
num=0.44;
denum=[0.001 , 0.05];
Tp2=tf(num, denum)
% -------------------------------------------------------------------
```

/E

Datasheet of the transformer's core.

Ferrites and accessories

ETD 39/20/13
Core and accessories

Series/Type: **B66363, B66364**

Date: May 2017

Core

- To IEC 62317-6
- For SMPS transformers with optimum weight/performance ratio at small volume
- Delivery mode: single units

Magnetic characteristics (per set)

$\Sigma l/A$ = 0.74 mm^{-1}
l_e = 92.2 mm
A_e = 125 mm^2
A_{min} = 123 mm^2
V_e = 11500 mm^3

FEK0053-8

Approx. weight 60 g/set

Ungapped
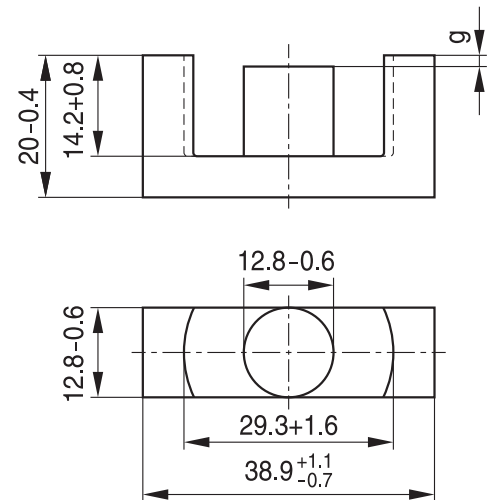
Material	A_L value nH	μ_e	B_S* mT	P_V W/set	Ordering code
N27	2550 +30/–20%	1500	320	< 2.22 (200 mT, 25 kHz, 100 °C)	B66363G0000X127
N87	2700 +30/–20%	1600	320	< 6.00 (200 mT, 100 kHz, 100 °C)	B66363G0000X187
N97	2800 +30/–20%	1650	320	< 5.10 (200 mT, 100 kHz, 100 °C)	B66363G0000X197

* H = 250 A/m; f = 10 kHz; T = 100 °C

Gapped (A_L values/air gaps examples)

Material	g mm	A_L value approx. nH	μ_e	Ordering code ** = 27 (N27) = 87 (N87)
N27, N87	0.10 ±0.02	1062	622	B66363G0100X1**
	0.20 ±0.02	639	374	B66363G0200X1**
	0.50 ±0.05	326	191	B66363G0500X1**
	1.00 ±0.05	196	115	B66363G1000X1**
	2.00 ±0.05	115	65	B66363G2000X1**

The A_L value in the table applies to a core set comprising one ungapped core (dimension g = 0 mm) and one gapped core (dimension g > 0 mm).

Other A_L values/air gaps and materials available on request — see Processing remarks on page 5.

Please read *Cautions and warnings* and
Important notes at the end of this document.

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Calculation factors (for formulas, see *"E cores: general information"*)

Material	Relationship between air gap – A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (100 °C)	K4 (100 °C)
N27	196	−0.734	308	−0.847	287	−0.865
N87	196	−0.734	300	−0.796	280	−0.873

Validity range: K1, K2: 0.10 mm < s < 3.00 mm
                          K3, K4: 90 nH < A_L < 850 nH

Coil former

Material: GFR polyterephthalate, UL 94 V-0, insulation class to IEC 60085:
                B66364B: F ≙ max. operating temperature 155 °C, color code black
                Valox 420-SE0 [E207780 (M)] SABIC JAPAN L L C
                B66364W: H ≙ max. operating temperature 180 °C, color code black
                Rynite FR 530® [E41938 (M)], E I DUPONT DE NEMOURS & CO INC
Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s
Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s
Winding: see Processing notes, 2.1

Yoke

Material: Stainless spring steel (0.4 mm)

Coil former					Ordering code
Sections	A_N mm^2	l_N mm	A_R value μΩ	Pins	
1	178	69	13.3	16	B66364B1016T001 B66364W1016T001
Yoke (ordering code per piece, 2 are required)					B66364A2000X000

Coil former   **Yoke**

FEK0491-A-E

FEK0492-I

Please read *Cautions and warnings* and
Important notes at the end of this document.

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/F
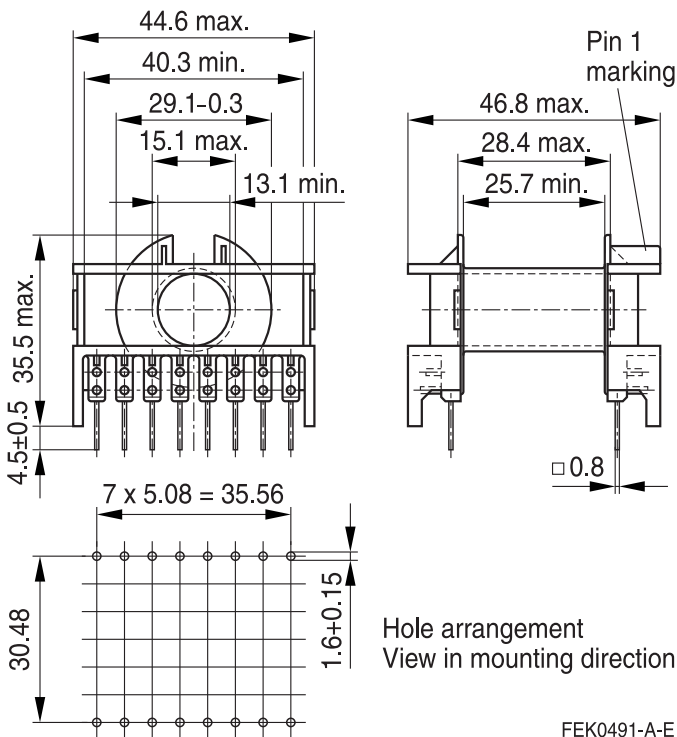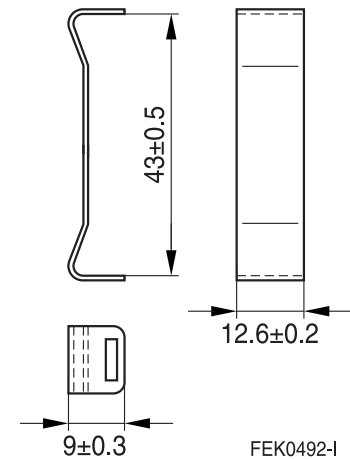
Datasheet of IPM50RSA120 and evaluation board.

PM50RSA120

**FLAT-BASE TYPE
INSULATED PACKAGE**

1. V UPC
2. UFo
3. Up
4. V UPI
5. V VPC
6. VFo
7. V P
8. V VPI
9. V WPC
10. WFo
11. WP
12. V WPI
13. V NC
14. V NI
15. B R
16. U N
17. V N
18. W N
19. Fo

Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	4.33±0.04	110.0±1.0
B	3.74±0.02	95.0±0.5
C	3.50±0.04	89.0±1.0
D	3.27	83.0
E	2.91±0.02	74.0±0.5
F	2.44	62.0
G	1.28	32.6
H	1.24	31.6
J	1.02	26.0
K	0.94	24.0
L	0.87 +0.06/-022.0 +1.5/-0.0	
M	0.79	20.0
N	0.76	19.4
P	0.75	19.0
Q	0.708	17.98
R	0.670	17.02

Dimensions	Inches	Millimeters
S	0.67	17.0
T	0.52	13.2
U	0.39	10.0
V	0.28	7.0
W	0.30	7.5
X	0.24	6.0
Y	0.24 Rad.	Rad. 6.0
Z	0.22 Dia.	Dia. 5.5
AA	Metric M5	M5
AB	0.127	3.22
AC	0.10	2.6
AD	0.08	2.0
AE	0.07	1.8
AF	0.06	1.6
AG	0.02±0.01	0.5±0.3

Description:

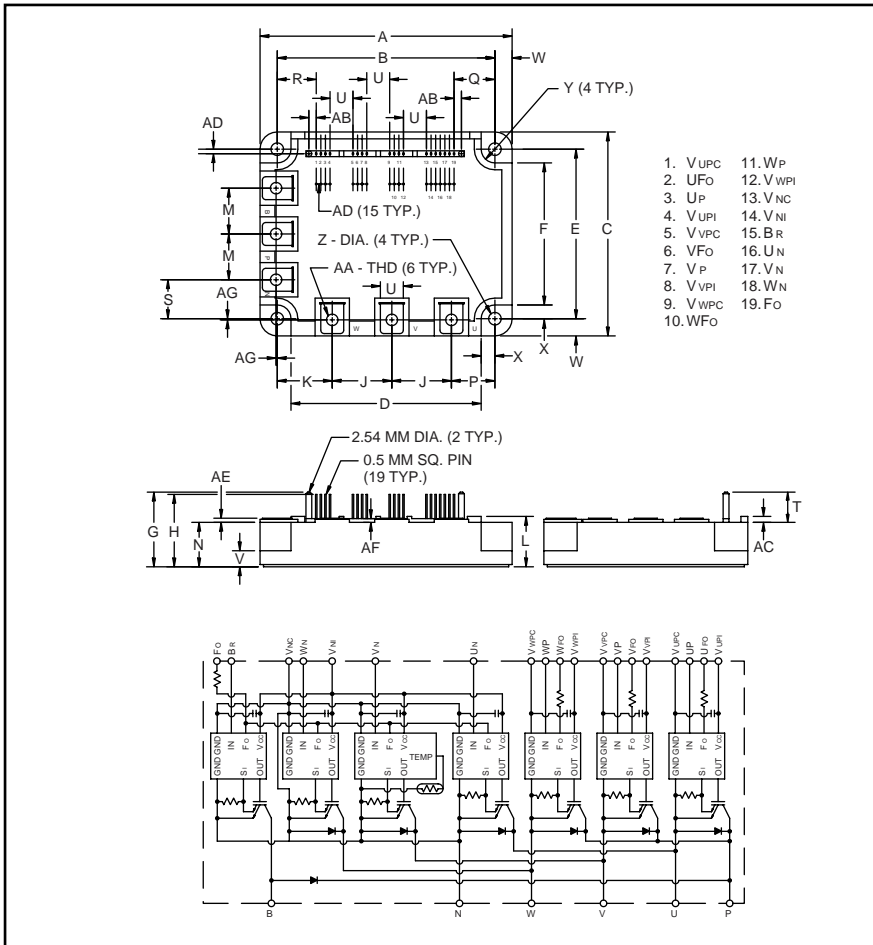Mitsubishi Intelligent Power Modules are isolated base modules designed for power switching applications operating at frequencies to 20kHz. Built-in control circuits provide optimum gate drive and protection for the IGBT and free-wheel diode power devices.

Features:

☐ Complete Output Power Circuit

☐ Gate Drive Circuit

☐ Protection Logic
 – Short Circuit
 – Over Current
 – Over Temperature
 – Under Voltage

Applications:

☐ Inverters
☐ UPS
☐ Motion/Servo Control
☐ Power Supplies

Ordering Information:

Example: Select the complete part number from the table below -i.e. PM50RSA120 is a 1200V, 50 Ampere Intelligent Power Module.

Type	Current Rating Amperes	V$_{CES}$ Volts (x 10)
PM	50	120

MITSUBISHI ELECTRIC

PM50RSA120

FLAT-BASE TYPE
INSULATED PACKAGE

Absolute Maximum Ratings, T_j = 25°C unless otherwise specified

	Symbol	Ratings	Units
Power Device Junction Temperature	T_j	-20 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Case Operating Temperature	T_C	-20 to 100	°C
Mounting Torque, M5 Mounting Screws	—	1.47 ~ 1.96	N · m
Mounting Torque, M5 Main Terminal Screw	—	1.47 ~ 1.96	N · m
Module Weight (Typical)	—	550	Grams
Supply Voltage Protected by OC and SC (V_D = 13.5 - 16.5V, Inverter Part, T_j = 125°C)	$V_{CC(prot.)}$	800	Volts
Isolation Voltage (Main Terminal to Baseplate, AC 1 min.)	V_{RMS}	2500	Volts

Control Sector

	Symbol	Ratings	Units
Supply Voltage (Applied between V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC})	V_D	20	Volts
Input Voltage (Applied between U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, $U_N \cdot V_N \cdot W_N \cdot B_r$-$V_{NC}$)	V_{CIN}	20	Volts
Fault Output Supply Voltage Applied between (U_{FO}-V_{UPC}, V_{FO}-V_{VPC}, W_{FO}-V_{WPC}, F_O-V_{NC})	V_{FO}	20	Volts
Fault Output Current (Sink Current at U_{FO}, V_{FO}, W_{FO} and F_O Terminal)	I_{FO}	20	mA

IGBT Inverter Sector

	Symbol	Ratings	Units
Collector-Emitter Voltage (V_D = 15V, V_{CIN} = 15V)	V_{CES}	1200	Volts
Collector Current, (T_C = 25°C)	I_C	50	Amperes
Peak Collector Current, (T_C = 25°C)	I_{CP}	100	Amperes
Supply Voltage (Applied between P - N)	V_{CC}	900	Volts
Supply Voltage, Surge (Applied between P - N)	$V_{CC(surge)}$	1000	Volts
Collector Dissipation	P_C	347	Watts

Brake Sector

	Symbol	Ratings	Units
Collector-Emitter Voltage	V_{CES}	1200	Volts
Collector Current, (T_C = 25°C)	I_C	15	Amperes
Peak Collector Current, (T_C = 25°C)	I_{CP}	30	Amperes
Supply Voltage (Applied between P - N)	V_{CC}	900	Volts
Supply Voltage, Surge (Applied between P - N)	$V_{CC(surge)}$	1000	Volts
Collector Dissipation	P_C	138	Watts
Diode Forward Current	I_F	15	Amperes
Diode DC Reverse Voltage	$V_{R(DC)}$	1200	Volts

MITSUBISHI ELECTRIC

Electrical and Mechanical Characteristics, $T_j = 25°C$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Control Sector						
Over Current Trip Level Inverter Part	OC	$-20°C \leq T \leq 125°C$, $V_D = 15V$	59	112	—	Amperes
Over Current Trip Level Brake Part			22	50	—	Amperes
Short Circuit Trip Level Inverter Part	SC	$-20°C \leq T \leq 125°C$, $V_D = 15V$	—	183	—	Amperes
Short Circuit Trip Level Brake Part			—	95	—	Amperes
Over Current Delay Time	$t_{off(OC)}$	$V_D = 15V$	—	10	—	μs
Over Temperature Protection	OT	Trip Level	111	118	125	°C
	OT_r	Reset Level	—	100	—	°C
Supply Circuit Under Voltage Protection	UV	Trip Level	11.5	12.0	12.5	Volts
	UV_r	Reset Level	—	12.5	—	Volts
Supply Voltage	V_D	Applied between V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	13.5	15	16.5	Volts
Circuit Current	I_D	$V_D = 15V$, $V_{CIN} = 15V$, V_{N1}-V_{NC}	—	44	60	mA
		$V_D = 15V$, $V_{CIN} = 15V$, V_{XP1}-V_{XPC}	—	13	18	mA
Input ON Threshold Voltage	$V_{th(on)}$	Applied between U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, $U_N \cdot V_N \cdot W_N \cdot B_r$-$V_{NC}$	1.2	1.5	1.8	Volts
Input OFF Threshold Voltage	$V_{th(off)}$		1.7	2.0	2.3	Volts
PWM Input Frequency	f_{PWM}	3-φ Sinusoidal	—	15	20	kHz
Fault Output Current	$I_{FO(H)}$	$V_D = 15V$, $V_{FO} = 15V$	—	—	0.01	mA
	$I_{FO(L)}$	$V_D = 15V$, $V_{FO} = 15V$	—	10	15	mA
Minimum Fault Output Pulse Width	t_{FO}	$V_D = 15V$	1.0	1.8	—	ms

MITSUBISHI ELECTRIC

PM50RSA120

FLAT-BASE TYPE
INSULATED PACKAGE

Electrical and Mechanical Characteristics, T_j = 25°C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
IGBT Inverter Sector						
Collector Cutoff Current	I_{CES}	$V_{CE} = V_{CES}$, T_j = 25°C	—	—	1.0	mA
		$V_{CE} = V_{CES}$, T_j = 125°C	—	—	10	mA
Emitter-Collector Voltage	V_{EC}	$-I_C$ = 50A, V_D = 15V, V_{CIN} = 5V	—	2.5	3.5	Volts
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_D = 15V, V_{CIN} = 0V, I_C = 50A	—	2.5	3.5	Volts
		V_D = 15V, V_{CIN} = 0V, I_C = 50A, T_j = 125°C	—	2.2	3.2	Volts
Inductive Load Switching Times	t_{on}		0.5	1.0	2.5	µs
	t_{rr}	V_D = 15V, V_{CIN} = 0 ↔ 15V	—	0.15	0.3	µs
	$t_{C(on)}$	V_{CC} = 600V, I_C = 50A	—	0.4	1.0	µs
	t_{off}	T_j = 125°C	—	2.0	3.0	µs
	$t_{C(off)}$		—	0.7	1.2	µs
Brake Sector						
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_D = 15V, V_{CIN} = 0V, I_C = 15A, T_j = 25°C	—	2.8	3.8	Volts
		V_D = 15V, V_{CIN} = 0V, I_C = 15A, T_j = 125°C	—	2.2	3.2	Volts
Diode Forward Voltage	V_{FM}	$-I_C$ = 15A, V_D = 15V, V_{CIN} = 5V	—	2.5	3.5	Volts
Collector Cutoff Current	I_{CES}	$V_{CE} = V_{CES}$, T_j = 25°C	—	—	1	mA
		$V_{CE} = V_{CES}$, T_j = 125°C	—	—	10	mA

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Thermal Characteristics

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Each Inverter IGBT	—	—	0.36	°C/Watt
	$R_{th(j-c)F}$	Each Inverter FWDi	—	—	1.0	°C/Watt
	$R_{th(c-f)Q}$	Each Brake IGBT	—	—	0.9	°C/Watt
	$R_{th(c-f)F}$	Each Brake FWDi	—	—	2.0	°C/Watt
Contact Thermal Resistance	$R_{th(c-f)}$	Case to Fin Per Module, Thermal Grease Applied	—	—	0.027	°C/Watt

Recommended Conditions for Use

Characteristic	Symbol	Condition	Value	Units
Supply Voltage	V_{CC}	Applied across P-N Terminals	0 ~ 800	Volts
	V_D	Applied between V_{UP1}-V_{UPC}, V_{N1}-V_{NC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}	15 ± 1.5	Volts
Input ON Voltage	$V_{CIN(on)}$	Applied between U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, $U_N \cdot V_N \cdot W_N \cdot B_r$-$V_{NC}$	0 ~ 0.8	Volts
Input OFF Voltage	$V_{CIN(off)}$		4.0 ~ V_D	Volts
PWM Input Frequency	f_{PWM}	Using Application Circuit	5 ~ 20	kHz
Minimum Dead Time	t_{dead}	Input Signal	≥ 3	μs

Sep.2000

MITSUBISHI ELECTRIC

L1S1-SERIES IPM

EVALUATION BOARD

(EVBL1S1XX)
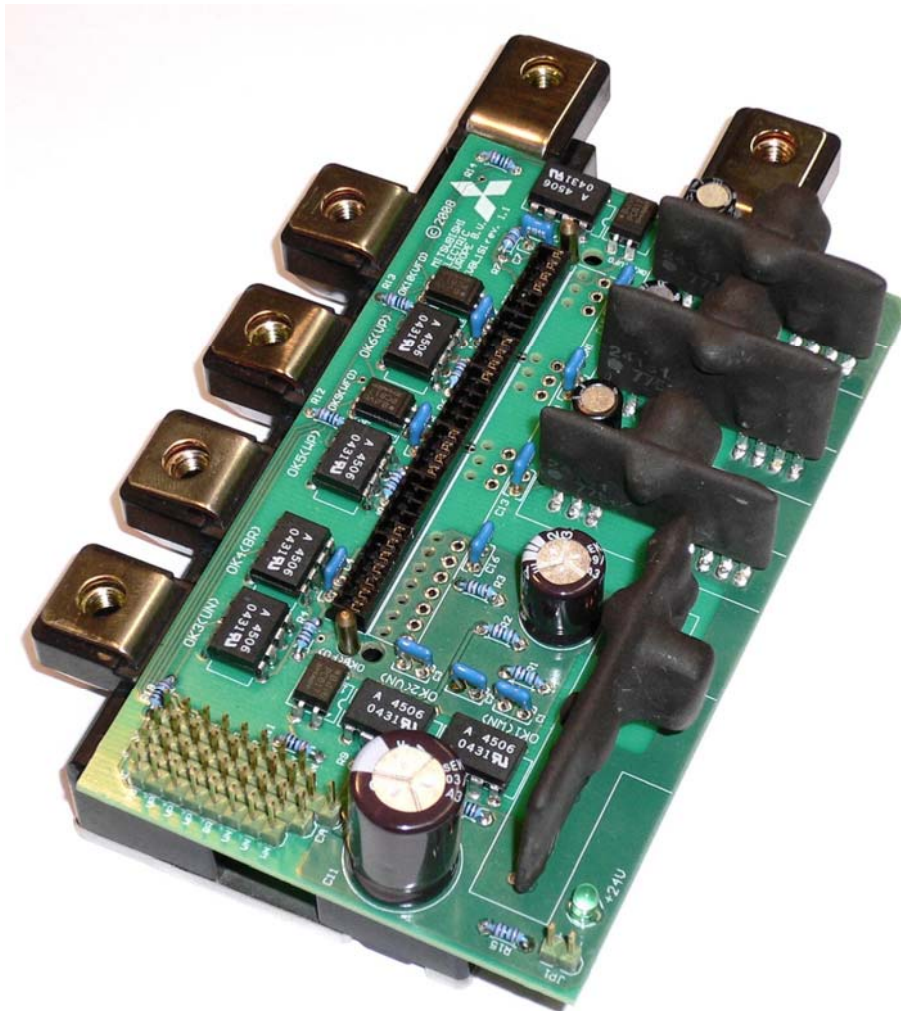
EVBL1S1 mounted on an L1-series IPM

(2.54mm connector (S1) not placed in this prototype)

Contens:

Caution: This evaluation board (EVB) is for testing purpose only. The evaluation board does not comply with any safety, isolation, environmental or EMI / EMC standard. Dangerous voltages can occur on the EVB and to equipment linked or connected to it. The operation should be carried out by qualified and authorized personnel only well respecting safety precautions.

1. Introduction

The L1S1-series IPM evaluation board is intended to functionally test the features and the performance of the Mitsubishi L1S1-series Intelligent Power Modules. The L1 and S1 series is using FULL Gate CSTBT IGBT technology. The series contains 600V and 1200V device with a current range from 25A up to 300A. The EVBL1S1XX evaluation board can be used with all devices of the L1 and S1 series. Two different IPM connectors allow to use both the S1 and L1 devices. The control terminal pin assignment of the board is compatible with High-Active and Low-Active control signals and realized with a standard 2,54mm pin-header. Such 2,54mm pin-headers are available as a world wide standard. Only one power supply with 24V and recommended minimum of 300mA supply current capability is necessary to supply the Evaluation Board including the control and driver part of the IPM. The employed DC-DC converters ensure that the Evaluation Board power supply is completely isolated from IPM power supply. The DC-DC converter form in conjunction with the photocouplers a safety insulation barrier between control input of the evaluation board and the IPM's logic and supply.

The Evaluation Board's circuit is based on the interface and supply circuit which is recommended in the L1 and S1 IPM datasheets.

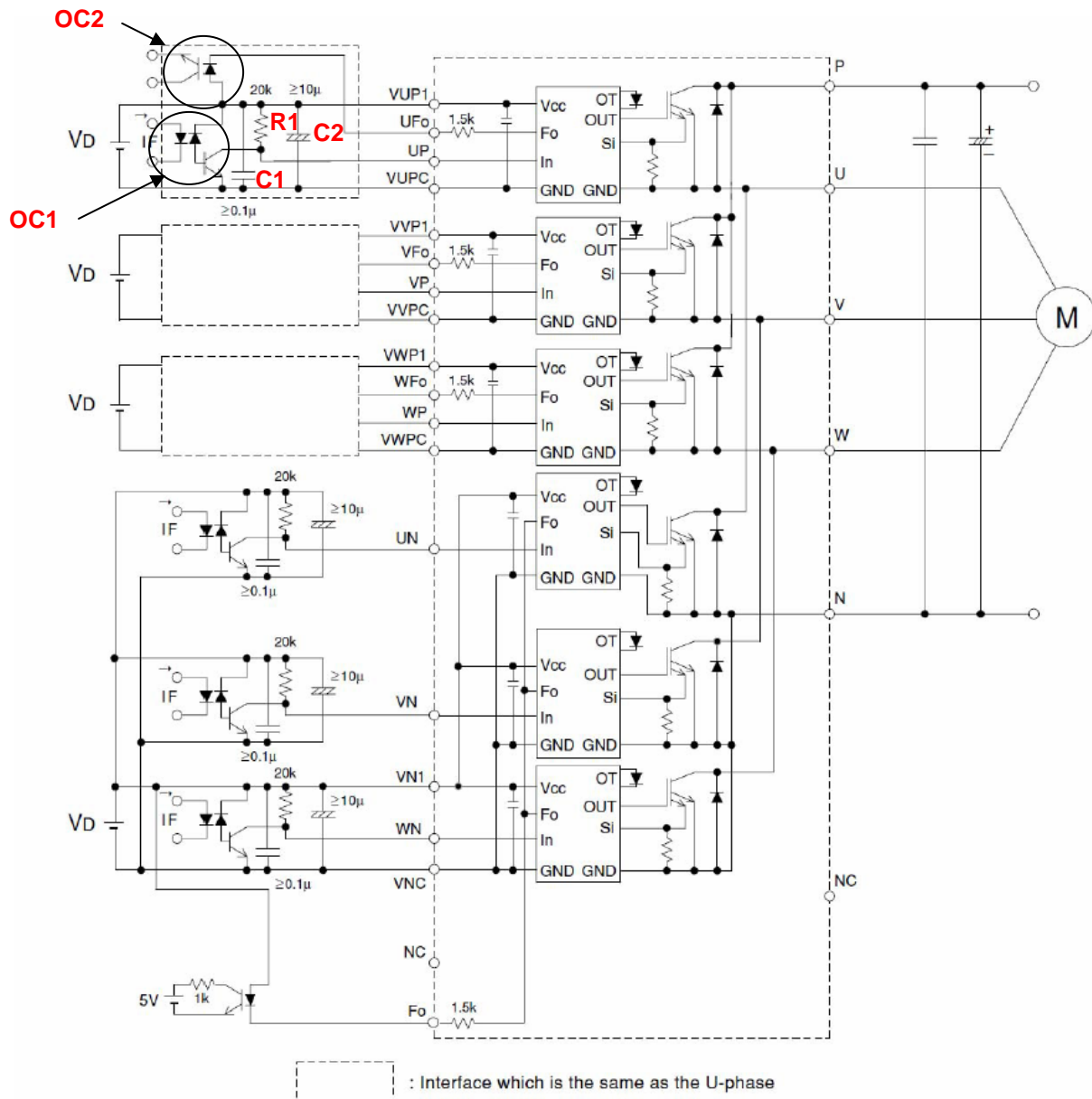## 1.1 Application Example Circuit from the Datasheet:

figure 1: recommended interface circuit to L1/S1 IPM

V_D = isolated supply 15V
OC1   = fast safety photocoupler with high dv/dt CMR and isolation capability
OC2   = safety photocoupler for FO , high isolation and safety (VDE)
C1   = fast ceramic HF-benching capacitor ≥ 100nF/50V
C2   = enery storage longlife low ESR electrolytic capacitor ≥ 10µF/35V, T_{max}=105°C
R1   = 18kΩ…20kΩ pull up resistor

The Evaluation Board contains the isolated power supply and interface to control the IPM. The IPM itself is not part of the EVBL1S1 and must be ordered separately. To operate the IPM device in a basic application the following minimum additional hardware and the load itself is required.

Figure 2 shows the essential functional blocks to make the test setup operable:

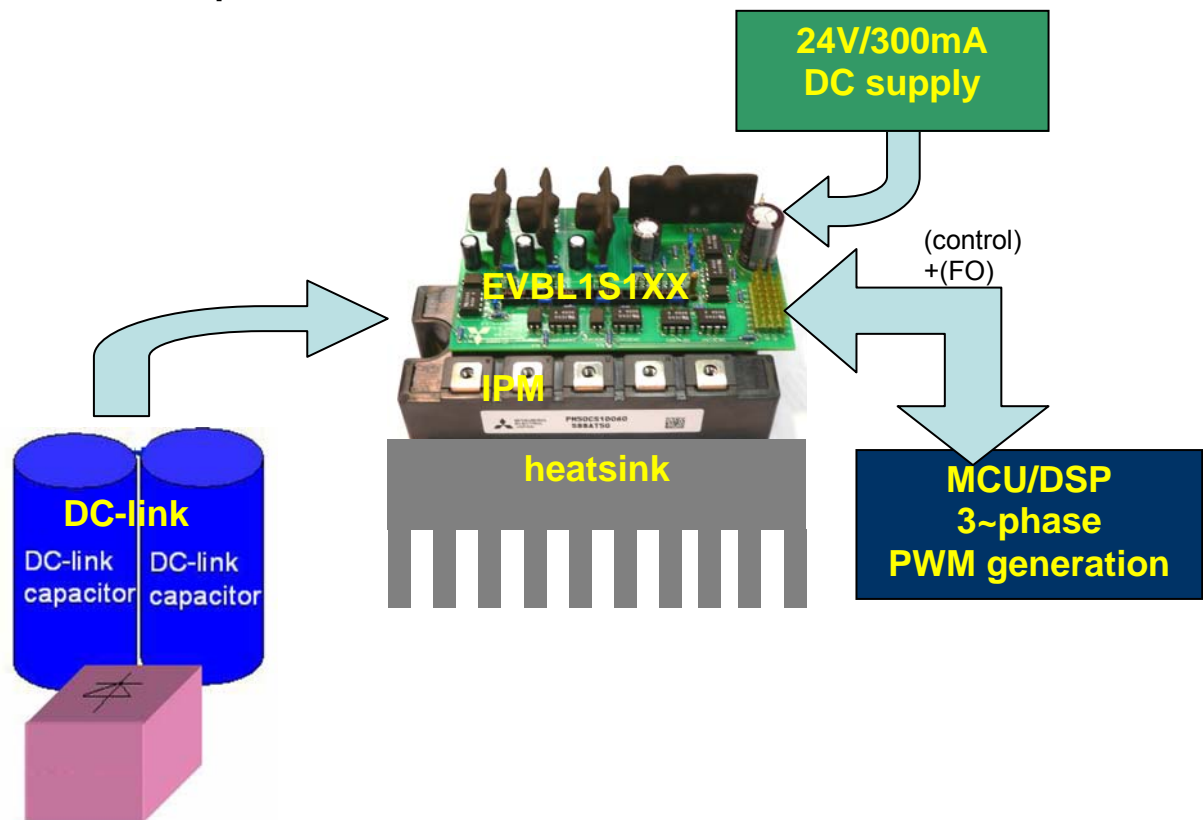## 1.2 Hardware requirements to use the IPM:

figure 2: EVBL1S1XX and required application hardware for minimum operational test

Further information about the hardware requirements are given in the application note "USING INTELLIGENT POWER MODULES.

(http://mitsubishichips.com/Global/files/manuals/powermos6_0.pdf)

2. Schematic of the Evaluation Board

Figure 3 is extracting the interface and supply circuit of the P-Side IGBT of leg U as an example of the structure of the entire board.
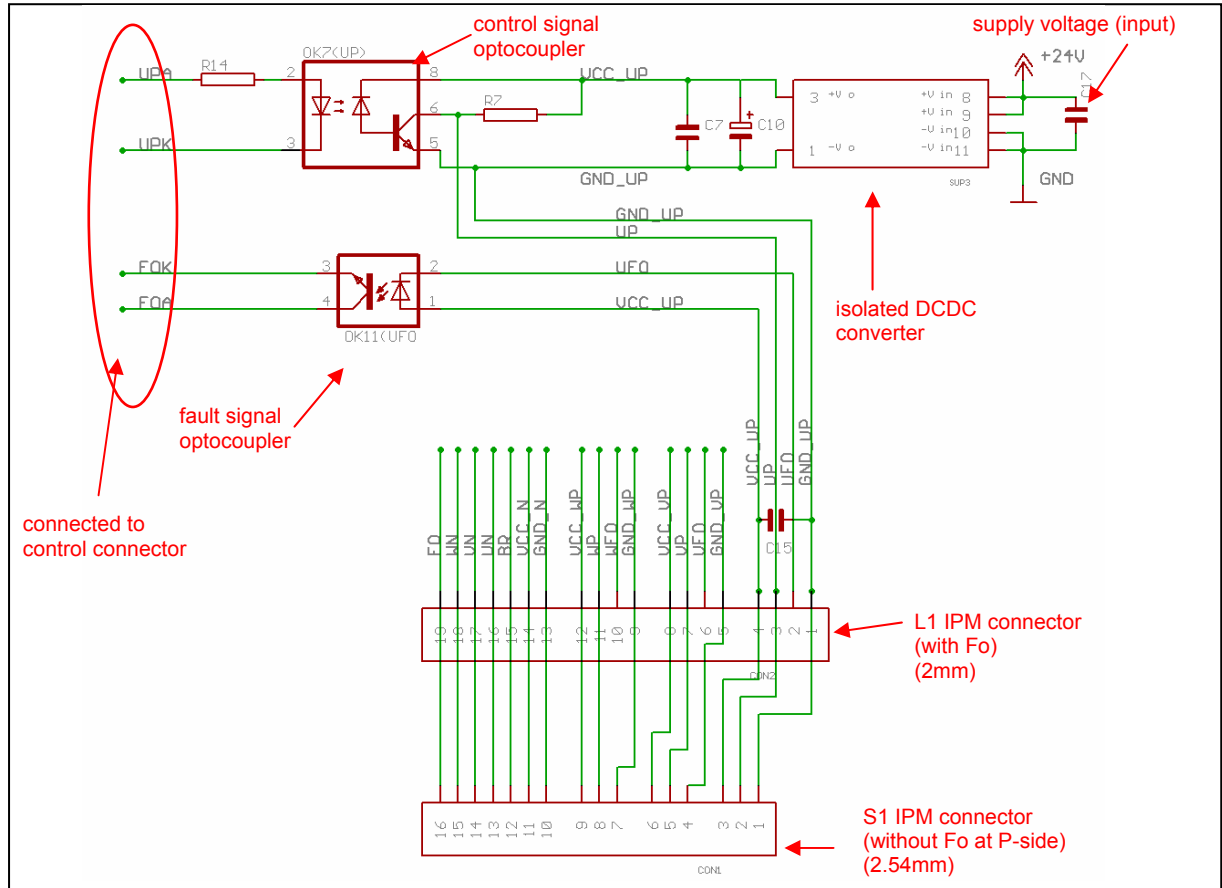
Schematic UP Interface:

figure 3: P-side phase"U"

A high speed optocoupler (OK7) with high common mode rejection (CMR) is used for the signal input. The input pull-up resistor (R7=18k…20kΩ) has been selected to be low enough to avoid noise pick-up and to be high enough in resistance to allow the high speed phototransistor with a CTR of ~ 35% to pull the IPM input below the recommended maximum $V_{CIN(on)}$ threshold voltage, e.g. to turn on the IPM safely. A low speed optocoupler with safety approval is used to transfer the fault outputs (Fo) of the IPM to the insulated side. Decoupling capacitors C7,C17 and C15 are used to avoid malfunctions caused by noise and C10, the electrolytic capacitor, provides the energy reservoir for the floating side. Such kind of noise is mainly created by the fast switching IGBTs and the resulting high dv/dt and di/dt.

The L1 and S1 connectors allow to use both IPM series and provide an easy installation of the evaluation board.

In figure 4 the complete evaluation board schematic is shown.
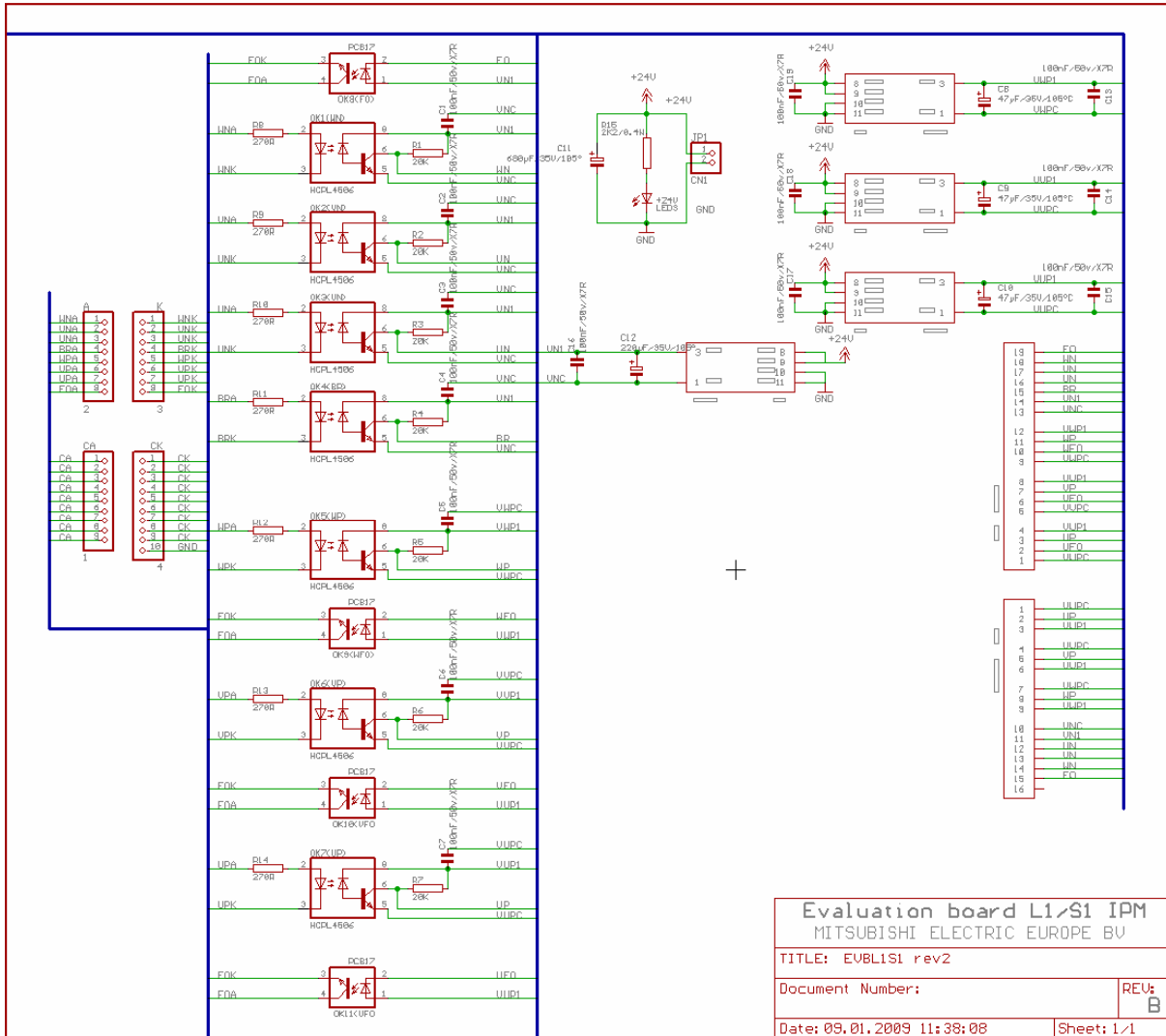
2.1 Schematic of the whole evaluation board:

figure 4: complete schematic of the evaluation board

The schematic according to figure 4 reveals the simplicity of the interface circuit to drive the IPM. Indeed by the high degree of integration in the IPM itself which provides the driver and complete protection functions like under voltage, over temperature sensor on each IGBT chip, the total external circuitry becomes simple.
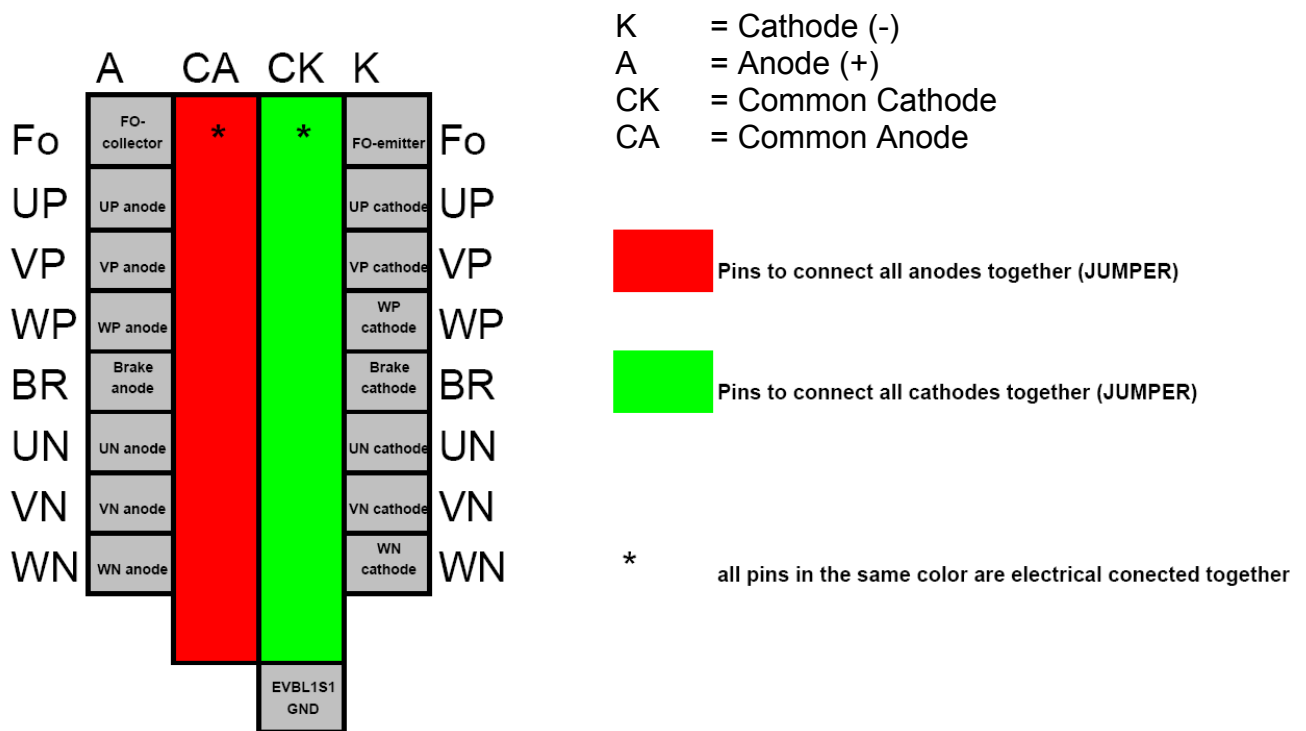
3. Control interface connector

The control terminal pin assignment of the board is compatible with High-Active and Low-Active control signals and realized with a standard 2,54mm pin-header array. The series resistor of the input high speed optocoupler diode is dimensioned as 270Ω for a recommended control input voltage of 5V.

All cathodes and anodes of the input high speed optocoupler are connected through these 270R resistances to the pin-header. The pin-header contains only one Emitter and Collector pin as a sum signal of all fault output phototransistors. The following examples describe how to connect the evaluation board for high active and low active PWM signals.

3.1 General connector description:
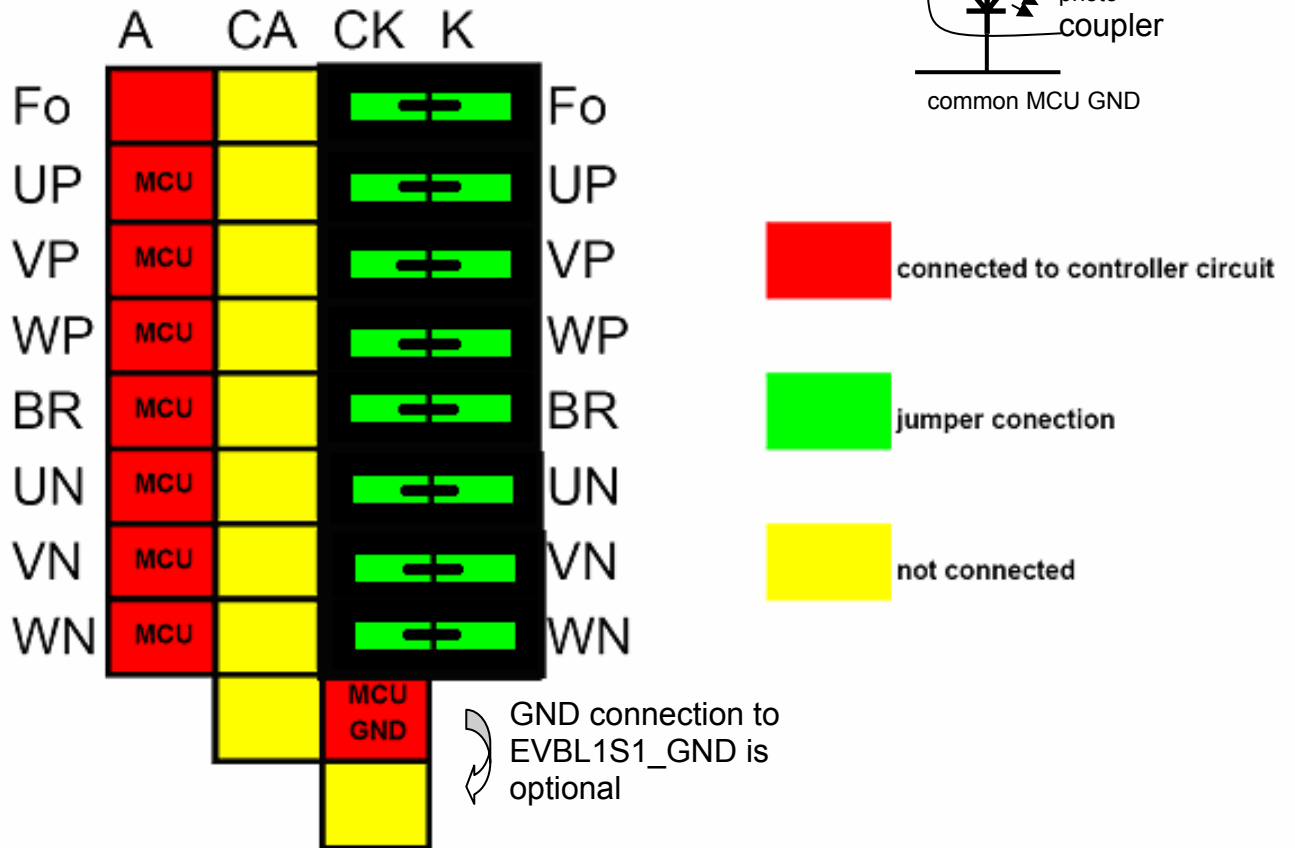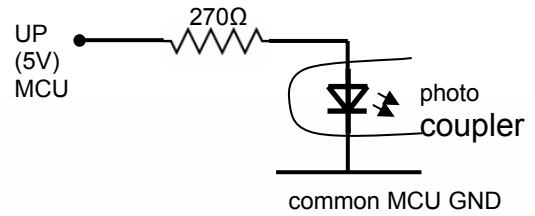

K = Cathode (-)
A = Anode (+)
CK = Common Cathode
CA = Common Anode

Pins to connect all anodes together (JUMPER)

Pins to connect all cathodes together (JUMPER)

*   all pins in the same color are electrical conected together

3.2 configuration for high active PWM:

"CK" is connected to "K" by jumpers.

example channel (UP):

UP (5V) MCU — 270Ω — photo coupler — common MCU GND

	A	CA	CK	K	
Fo					Fo
UP	MCU				UP
VP	MCU				VP
WP	MCU				WP
BR	MCU				BR
UN	MCU				UN
VN	MCU				VN
WN	MCU				WN
			MCU GND		

GND connection to EVBL1S1_GND is optional

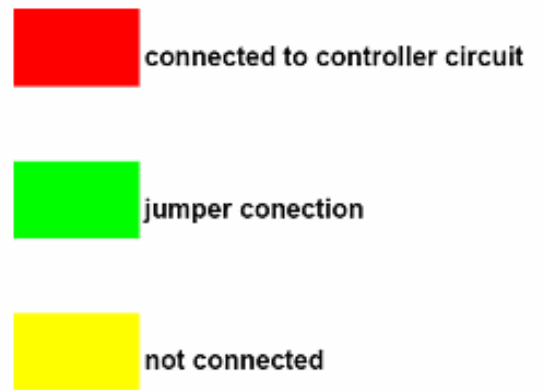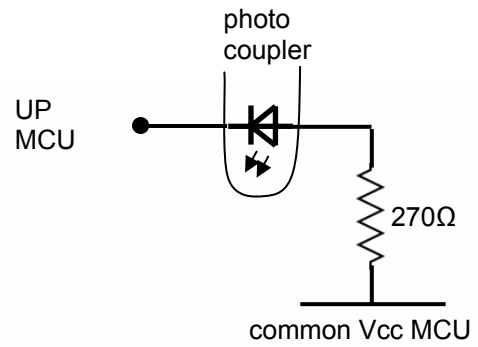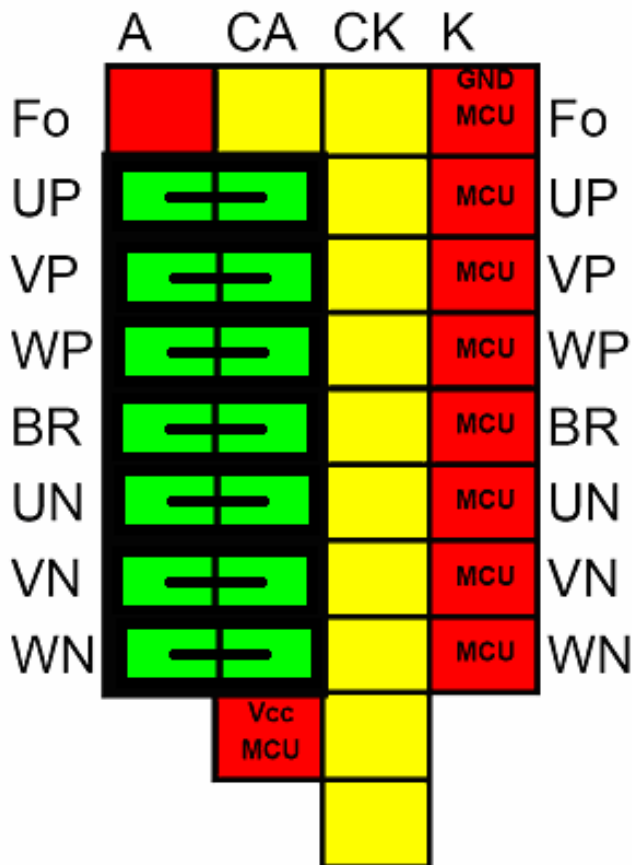connected to controller circuit

jumper conection

not connected

3.3. Configuration for low active PWM example:

"CA" is connected to "A" by jumpers.

example channel (UP):

/G

Simulink algorithm of the designed controller (for interfacing through dSPACE 1202 and ControlDesk software).

RTI Data

The designed controller with two PI controller, two input signal measurements, and signal generation units.

5e-5
Sm_Ts

[D_Smain]
Duty cycle, main switches

Period
Duty Cycle
Main Switch pulse generator

2.5e-5
Saux_Ts

0.2
D_Saux

Period
Duty Cycle
Aux Switch pulse generator

1
V,out_ref

[V_out]
V,out_measured

1
reset

[i_in]
i,in_measured

V,out_ref
V,out_measured
Reset
i,in_ref
voltage controller

i,in_ref
i,in_measured   D_Smain
Reset
current controlller

[D_Smain]

ADC CL1
Channel: 1
ADC

50
input gain

10
V_out measured

[V_out]

ADC CL1
Channel: 2
ADC

ADC_CLASS1_BL2

1
input gain1

10
i_in measured

[i_in]