Cascaded Model Predictive Control of Grid Connected Converter with LCL Filter

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***Abstract*—This paper presents a control strategy for grid connected voltage source converters with LCL filter, based on a cascade of two model predictive controllers (MPC). Despite the attention MPC has received in the research community over the last years, there are still raised question about what advantages such control methods can offer, compared to existing established control strategies. The cascaded MPC control algorithm is therefore implemented in a low-cost embedded system, to verify its commercial viability. This is made possible due to recent development in system-on-chip devices. Simulations and experimental results are presented to show the expected performance.**

***Index Terms*—LCL filter, model predictive control, power conversion, power electronics, voltage source converter.**

I. Introduction

Power electronic converters have developed to be important devices, not only in consumer products, but also for distributing and controlling power in the electric power grid. Especially in the area of connecting renewable energy to the grid, power electronics has proven itself indispensable. Performance and efficiency of the converter highly depends on the control algorithm, motivating a search for improvements utilizing the increasing computational power of low-cost microcontrollers and field-programmable gate arrays (FPGAs).

For controlling two-level voltage source converters (VSC) such as the one presented in Fig. 1, a whole range of different control methods has been proposed over the years [1]. Voltage oriented control (VOC) has been one of the established control methods for several decades, due to its simple construction and low computational requirements [2]. Recently, more computational demanding control methods, such as model predictive control (MPC), has been considered as a way to improve control performance in VSCs [3].

MPC originates from the 1970s chemical industry, where it was used to optimize plants with a large number of inputs and outputs [4]. Based on a mathematical model of the plant, future behavior of the system is predicted a certain time into the future, called prediction horizon. Since all systems are subjected to model uncertainty and disturbances, the optimization and predictions are recalculated at every time step, known as moving horizon. This introduces a sort of feedback to the control system. In control of power electronics, two different main approaches to MPC has been developed; finite control set MPC (FCS-MPC) [5] and continuous control set MPC (CCS-MPC) [1].

In FCS-MPC, the switched nature of the converter is utilized. With a finite number of possible solutions to the control problem, optimization is as simple as calculating all possibilities and pick the one with lowest cost/error. The method is simple and easy to implement, but the number of solutions increase exponentially with the prediction horizon and is therefore kept short, in most cases only as a one-step prediction.

A completely different approach is used in CCS-MPC, where the mathematical model of the converter is a continuous system. The switched nature of the converter is not included in the model, which results in an infinite number of solutions. Optimal solution can be found by using classic optimization theory, such as convex optimization [6-8]. The actual gate signals for the power transistors are usually generated using a modulator [1, 9-11], or with a secondary inner controller [12].

All grid-connected VSC needs a filter to smooth out the square wave voltage from the converter to a sinusoidal current applied to the grid. While this used to be an L filter, a more modern approach is to use LCL filters, which is a more compact higher order filter. While the LCL filter allows the use of smaller and cheaper components, the filter is subjected to resonance phenomena between the inductive and capacitive elements. This brings an additional challenge to the control strategy, which has been analyzed in [13]. Since passive damping of the oscillations in the filter results in power losses and lower efficiency, commercial solutions should be based on an active damping algorithm integrated in the converter control strategy.

MPC applied to VSC with active damping of LCL filters, has not received the same attention as the L filter case, most likely due to the increased complexity of the control algorithm. Algorithms based on FCS-MPC are, with the exception of [14], not able to dampen resonance in the LCL filter as an inherent property of the MPC, but require an additional damping algorithm. The reason being that the prediction horizon is too short to detect and dampen the oscillations.

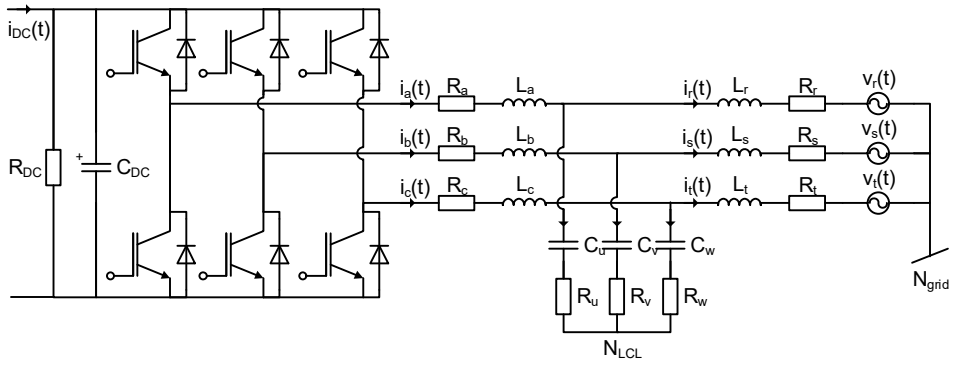

Fig. 1. Grid connected two-level three-phase converter with LCL filter

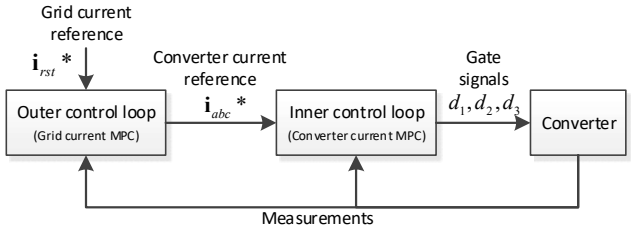

Fig. 2. Cascaded model predictive control

In [15, 16], a filter is used to suppress resonance frequencies form the filter, while [17, 18] implements a virtual resistor approach. An overview of different damping algorithms and feedback strategies can be found in [11].

Control algorithms based on CCS-MPC uses established optimization theory and are able to implement a longer prediction horizon, due to longer time-steps made possible by the modulator. Damping of the resonance in the LCL filter as an inherent property of the MPC algorithm is therefore more easily achieved, as demonstrated in [19]. While active damping does not require an additional damping algorithm, the fast response from FCS-MPC is lost.

A possible solution to this was proposed in [12], where CCS-MPC is used together with a FCS-MPC in cascade, replacing the modulator. The paper did not present a fully implemented solution nor any experimental results.

This paper presents an implementation version of the cascaded MPC concept presented in [12], based on the work in [20]. Simulations together with experimental results verifies the method, while implementation in low-cost hardware shows it as a commercial viable solution.

II. Cascaded Model Predictive Control

The cascaded MPC (CMPC) proposed in [12] is based on the fact that currents on the converter side of the filter changes faster than the grid side currents, with respect to the changes in the converter switches. This resembles a classic cascaded control case, where the control problem is divided into two parts as shown in Fig. 2: converter current control and grid current control. The following two subsections describes the improved version for each of the two MPCs.

A. Inner Control Loop (Converter current MPC)

The inner control loop handles the converter side currents, which changes fast. Since a short time-step is required and transistor gate signals should be generated, FCS-MPC is chosen as the most suitable control method. The FCS-MPC algorithm solves the following optimization problem:

$$\begin{aligned} \min_{d_1,d_2,d_3} \quad & \left\| \mathbf{i}_{abc}* - \mathbf{y}_{k+1} \right\|_2^2 \\ s.t. \quad & \mathbf{x}_{k+1} = A(d_1,d_2,d_3)\mathbf{x}_k \\ & \mathbf{y}_{k+1} = C\mathbf{x}_{k+1}, \end{aligned} \tag{1}$$

where $\mathbf{i}_{abc}*$ are the converter current references and $\mathbf{y}_{k+1}$ are the predicted converter currents.

The optimization is based on a subset of the continuous state-space model from [21], regarding the converter side currents:

$$A_{1,2} = \begin{bmatrix} -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & \frac{-1}{L_{abc}} & 0 & \frac{2d_1(t)-d_2(t)-d_3(t)}{3L_{abc}} \\ 0 & -\frac{R_{abc}}{L_{abc}} & 0 & 0 & 0 & \frac{-1}{L_{abc}} & \frac{-d_1(t)+2d_2(t)-d_3(t)}{3L_{abc}} \end{bmatrix},$$
$$\mathbf{x} = \begin{bmatrix} i_a(t) & i_b(t) & i_r(t) & i_s(t) & v_{Cu}(t) & v_{Cv}(t) & V_{DC}(t) \end{bmatrix}^T, \tag{2}$$

where R_{abc} is the internal resistance of the converter side inductors, L_{abc} is the converter side inductance; and $d_1(t)$, $d_2(t)$ and $d_3(t)$ are the switching signals for each of the three legs in the converter. The state vector $\mathbf{x}$ holds the state variables for converter, as shown in Fig. 1.

The continuous system in (2) is manually discretized using zero order hold before being applied in (1).

B. Outer Control Loop (Grid Current MPC)

The outer control loop handles the grid side currents, which changes more slowly in respect to voltage changes due to transistor switching. A CCS-MPC algorithm is therefore chosen for this controller. Since the inner control loop generates the actual transistor gate signals, this controller can implement both longer time-step and longer prediction horizon. The mathematical model is based on a subset of [21]. The state-space system incorporate integral action by using an

augmented state-vector, where $\Delta\mathbf{u}_k$ is used as the input vector:

$$\begin{bmatrix}\mathbf{x}_{k+1}\\ \mathbf{u}_k\end{bmatrix}=\underbrace{\begin{bmatrix}A & B\\ 0 & I\end{bmatrix}}_{\hat{A}}\underbrace{\begin{bmatrix}\mathbf{x}_k\\ \mathbf{u}_{k-1}\end{bmatrix}}_{\hat{\mathbf{x}}}+\underbrace{\begin{bmatrix}B\\ I\end{bmatrix}}_{\hat{B}}\Delta\mathbf{u}_k+\underbrace{\begin{bmatrix}F\\ 0\end{bmatrix}}_{\hat{F}}\mathbf{v}_k. \tag{3}$$

The state-vector $\mathbf{x}(t)$ and disturbance vector $\mathbf{v}(t)$ are defined as:

$$\begin{aligned}\mathbf{x}(t)&=\begin{bmatrix}i_r(t) & i_s(t) & v_{Cu}(t) & v_{Cv}(t)\end{bmatrix}^T,\\ \mathbf{v}(t)&=\begin{bmatrix}v_r(t) & v_s(t) & v_t(t)\end{bmatrix}^T,\end{aligned} \tag{4}$$

while the matrices in (3) have been derived as:

$$A=\begin{bmatrix}-\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}} & 0\\ 0 & -\frac{R_{rst}}{L_{rst}} & 0 & \frac{1}{L_{rst}}\\ -\frac{1}{C_{uvw}} & 0 & 0 & 0\\ 0 & -\frac{1}{C_{uvw}} & 0 & 0\end{bmatrix},\quad B=\begin{bmatrix}0 & 0\\ 0 & 0\\ \frac{1}{C_{uvw}} & 0\\ 0 & \frac{1}{C_{uvw}}\end{bmatrix},$$
$$F=\begin{bmatrix}-\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}} & \frac{1}{3L_{rst}}\\ \frac{1}{3L_{rst}} & -\frac{2}{3L_{rst}} & \frac{1}{3L_{rst}}\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix},\quad C=\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\end{bmatrix}. \tag{5}$$

Prediction of future values is a key part of the MPC algorithm. Based on the state-space system in (3), future values to be controlled can be expressed based on the procedure from [8] as:

$$\underbrace{\begin{bmatrix}\mathbf{y}_{k+1}\\ \mathbf{y}_{k+2}\\ \vdots\\ \mathbf{y}_{k+n}\end{bmatrix}}_{\underset{\rightarrow k}{\mathbf{y}}}=\underbrace{\begin{bmatrix}\hat{C}\hat{A}\\ \hat{C}\hat{A}^2\\ \vdots\\ \hat{C}\hat{A}^n\end{bmatrix}}_{P}\hat{\mathbf{x}}_k+\underbrace{\begin{bmatrix}\hat{C}\hat{B} & 0 & \cdots\\ \hat{C}\hat{A}\hat{B} & \hat{C}\hat{B} & \cdots\\ \vdots & \vdots & \cdots\\ \hat{C}\hat{A}^{n-1}\hat{B} & \hat{C}\hat{A}^{n-2}\hat{B} & \cdots\end{bmatrix}}_{H}\underbrace{\begin{bmatrix}\Delta\mathbf{u}_k\\ \Delta\mathbf{u}_{k+1}\\ \vdots\\ \Delta\mathbf{u}_{k+n-1}\end{bmatrix}}_{\Delta\underset{\rightarrow k-1}{\mathbf{u}}}+$$
$$\underbrace{\begin{bmatrix}\hat{C}\hat{F} & 0 & \cdots\\ \hat{C}\hat{A}\hat{F} & \hat{C}\hat{F} & \cdots\\ \vdots & \vdots & \cdots\\ \hat{C}\hat{A}^{n-1}\hat{F} & \hat{C}\hat{A}^{n-2}\hat{F} & \cdots\end{bmatrix}}_{Q}\underbrace{\begin{bmatrix}\mathbf{v}_k\\ \mathbf{v}_{k+1}\\ \vdots\\ \mathbf{v}_{k+n-1}\end{bmatrix}}_{\underset{\rightarrow k-1}{\mathbf{v}}}. \tag{6}$$

From (6), the cost function to be optimized is set as the squared 2-norm of the difference between reference values and the predicted system outputs:

$$J=\left\|\underset{\rightarrow k}{\mathbf{i}_{rst}}{}^*-\underset{\rightarrow k}{\mathbf{y}}\right\|_2^2=\left\|\underset{\rightarrow k}{\mathbf{i}_{rst}}{}^*-P\hat{\mathbf{x}}_k-H\Delta\underset{\rightarrow k-1}{\mathbf{u}}-Q\underset{\rightarrow k-1}{\mathbf{v}}\right\|_2^2. \tag{7}$$

The control problem is solved my minimizing the cost function in (7) as a convex optimization problem using quadratic programming:

$$\begin{aligned}\min_{\Delta\underset{\rightarrow k-1}{\mathbf{u}}}.\quad & \frac{1}{2}\Delta\underset{\rightarrow k-1}{\mathbf{u}}{}^T H^T H\Delta\underset{\rightarrow k-1}{\mathbf{u}}+\Delta\underset{\rightarrow k-1}{\mathbf{u}}{}^T g\\ s.t.\quad & \Delta\mathbf{u}_{lb}\le\Delta\underset{\rightarrow k-1}{\mathbf{u}}\le\Delta\mathbf{u}_{ub},\end{aligned} \tag{8}$$

where $g=H^T\left(P\hat{\mathbf{x}}_k+Q\underset{\rightarrow k-1}{\mathbf{v}}-\underset{\rightarrow k}{\mathbf{i}_{rst}}{}^*\right)$.

III. Implementation

The improved CMPC algorithm is implemented on a Microzed development board, featuring a Xilinx ZynQ device, which contains both a dual core ARM Cortex™-A9 microprocessor and programmable logic based on an Artix-7 FPGA.

One core of the microprocessor is dedicated to run the CCS-MPC algorithm for the outer control loop, with hardware acceleration of matrix-vector multiplications in the programmable logic. An active set-based algorithm is used to solve the control problem in (8) and can solve four iterations within 93 µs. Due to the tough timing constraints of the FCS-MPC algorithm, the inner control loop is fully implemented in the programmable logic. Both control loops compensate computational delay by predicting state-variables one step into the future, before running the actual control algorithm.

Reference current amplitude and phase shift is calculated based on active and reactive power reference (P*, Q*), together with knowledge of the grid phase-voltage amplitude $\hat{v}_r$:

$$\hat{i}_r=\frac{\sqrt{(P^*)^2+(Q^*)^2}}{\hat{v}_r}\cdot\frac{2}{3}, \tag{9}$$

$$\angle i_r=\arctan\left(\frac{-Q^*}{P^*}\right). \tag{10}$$

Based on the calculated amplitude and phase-shift in (9)-(10), the instantaneous grid current reference for the outer control loop is calculated on-line as shown in (11).

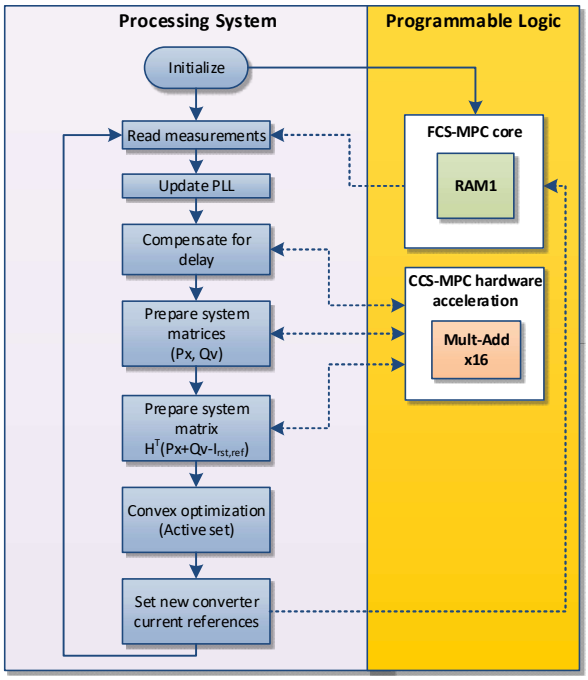

Fig. 3. Cascaded MPC implementation

TABLE I
IMPLEMENTATION PARAMETERS

Symbol	Parameter	Value
C_{DC}	DC-link capacitance	2200 µF
R_{DC}	DC-link resistive load	17 kΩ
L_{abc}	Converter side inductance	1 mH
R_{abc}	Converter side resistance	0.02 Ω
C_{uvw}	LCL filter capacitance	10 µF
L_{rst}	Grid side inductance	5 mH
R_{rst}	Grid side resistance	0.05 Ω
t_d	Transistor dead-time	5 µs
$T_{CCS\text{-}MPC}$	CCS-MPC time-step	100 µs
$T_{FCS\text{-}MPC}$	FCS-MPC time-step	5 µs
f_S	Sample frequency	200 kHz
N	Prediction horizon (CCS-MPC)	5
Δu_{lb}	Lower limit of Δu_{lb}	-2 A
Δu_{ub}	Upper limit of Δu_{lb}	2 A

$$i_r^* = \hat{i}_r \cdot \sin(\theta + \angle i_r), \quad i_s^* = \hat{i}_r \cdot \sin(\theta + \angle i_r - 2\pi/3), \tag{11}$$

where θ is the voltage angle in radians from a phase-locked-loop (PLL).

Parameters for the implementation are shown in Table I, while an overview of the implementation is shown in Fig. 3.

Stability of the algorithm is ensured by differentiate the time-step between outer and inner control loop by a factor of 10 or more, where the inner control loop is the fastest one in accordance with traditional design criteria for cascaded control. A terminal constraint is introduced to further improve the stability as suggested in [22], by forcing the step length to zero at the end of the prediction horizon, $\Delta \mathbf{u}_{N-1}$.

Active damping of the resonance phenomena in the LCL filter is achieved by selecting the prediction horizon long enough to detect the oscillations, in this case 500 µs, which includes 36% of the 1406 ms resonance period.

IV. SIMULATIONS

Simulations are performed in MATLAB/Simulink based on the same parameters as given in TABLE I and the two-level three-phase VSC model from [23]. Simulation time-step is set to 1 µs, while each MPC is placed in a triggered sub-system running at 100 µs and 5 µs for outer and inner control loop, respectively. Each controller has a computational delay of one time-step, which is compensated by predicting one additional step into the future using the same discrete state-space system as for MPC. The converter model is connected to a simulated stiff grid with phase-to-phase voltage of 230V RMS at 50 Hz.

The simulation results are shown in Fig. 4 and Fig. 5, where the CMPC algorithm is activated at t = 0.02s. The simulations are performed with two different dead-times between upper and lower transistor: 1µs that represents a converter with modern fast switching silicon carbide (SiC) transistor, and 5µs that represents an ordinary IGBT-based converter.

With 1µs dead-time as in Fig. 4, there is a close match between references and simulated values with THD = 2.47%. For full load condition, the THD is expected to be lower. Average switching frequency is simulated to 38 kHz, which is within recommended operating limits for available SiC devices.

As dead-time increases to 5µs, large deviation occurs around the peaks, increasing harmonic distortion to THD = 6.07%. The error is present, since large dead-time causes wrong predictions in the computational delay compensation by the FCS-MPC inner control loop. By utilizing knowledge of the dead-time when compensation for delay, error and THD can be reduced as shown in Fig. 7. However, average switching frequency is simulated to 60-70 kHz, which will result in increased switching losses.

To investigate the algorithms performance with model error due to inaccurate component parameters, simulations were performed where inductances and capacitances in the LCL filter was changed within ± 20% of their nominal values. The simulated grid currents summarized in Table II.

, only shows minor changes in performance due to parameter variation.

V. EXPERIMENTAL RESULTS

The CMPC algorithm were implemented in a Microzed development board in section III. This is now used in an experimental setup with an IGBT-based two-level three-phase VSC. Grid phase-to-phase voltage is set to 120 V RMS at 50 Hz, while the remaining parameters is equal to Table I.

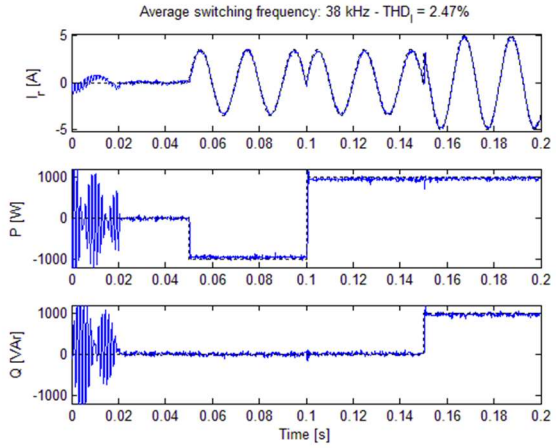

Fig. 4. Simulation with 1µs dead-time. References in dashed lines.

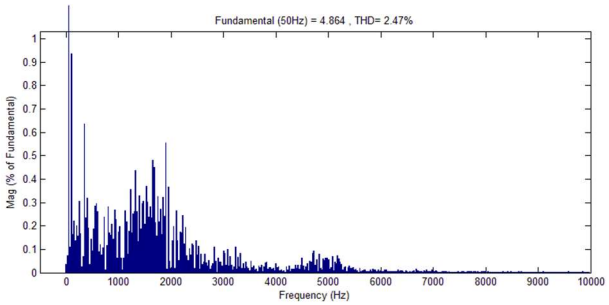

Fig. 6. Simulated grid current spectrum with 1µs dead-time, P* = 1000 W and Q* = 1000 VAr

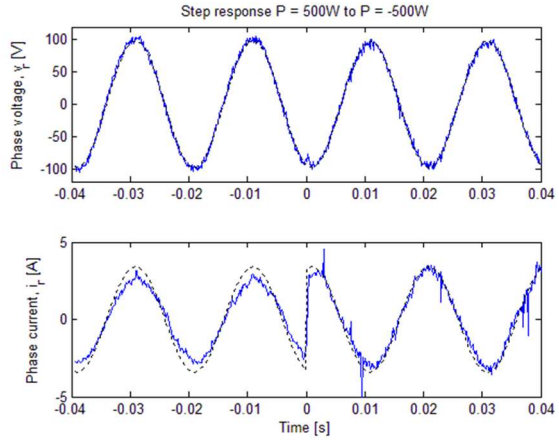

Fig. 8. Experimental step-response results with 5µs dead-time. Reference as dashed lines.

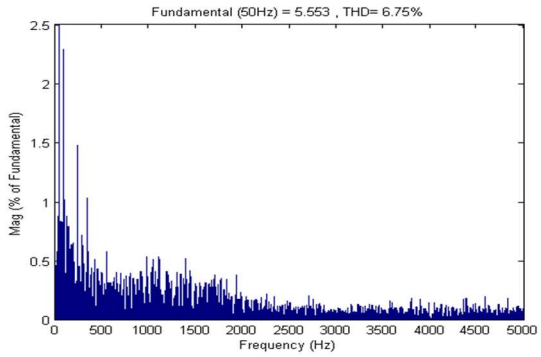

Fig. 9. Experimental grid current spectrum with 5µs dead-time

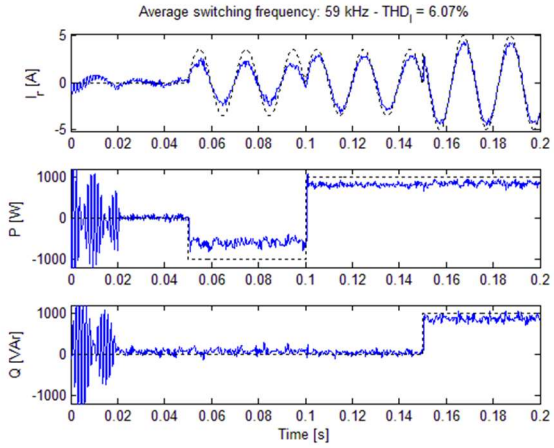

Fig. 5. Simulation with 5µs dead-time. References in dashed lines.

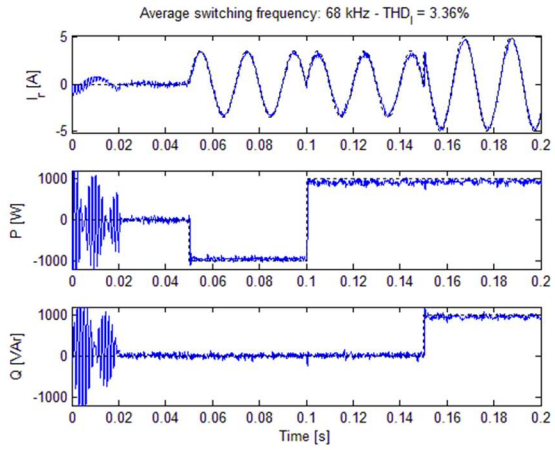

Fig. 7. Simulation with 5µs dead-time and dead-time compensation

TABLE II
MEAN AND STD OF ABSOLUTE ERROR WITH 3µS DEAD-TIME AT FULL LOAD

Case	Mean |e| [A]	STD [A]	THD [%]
Nominal	*1.03*	*0.61*	*2.12*
$1.2L_{abc}$	1.00	0.58	2.10
$0.8L_{abc}$	1.07	0.61	1.77
$1.2L_{rst}$	1.19	0.67	1.99
$0.8L_{rst}$	0.86	0.51	2.01
$1.2C_{uvw}$	0.99	0.58	2.12
$0.8C_{uvw}$	1.21	0.76	3.14

The DC-link is energized to 200 V DC using a rectifier connected to a variable AC source, where R_{DC} keeps the voltage from increasing in rectifying mode (negative power). Measurements are recorded using an Agilent DSO-X 2004A oscilloscope, before transferred to MATLAB as CSV (comma-separated values) files. Each measurement series consist of 2000 samples with a sampling time of 50 µs. Measurements are presented as recorded, without any filtering.

In Fig. 8, phase voltage and grid current are shown while the converter supplies 500 W to the grid. When analyzing the grid current, it is not able to follow its reference close to the peaks. This is the same behavior observed during simulations in Fig. 5. Dead-time has therefore a similar effect in both simulations

and experiments. The grid current spectrum in Fig. 9 shows an overall higher level of harmonic frequencies, where an increase in harmonics are observed in the range 1-2 kHz, comparable to the simulation in Fig. 6. THD of 6.75% from the experiment is slightly higher than the simulated 6.07%. Considering that measurement noise was not included in the simulation, there is a good match between simulated and experimental THD.

The step-response in Fig. 8 demonstrates the algorithms ability to adjust quickly when a new reference is set. The rate of change in the grid current is limited by the low-pass characteristic of the LCL filter and DC-link voltage.

While the simulations in section IV already established that CMPC is not suited for IGBT-based converters, the experiments verifies the simulations, given similar conditions. One can therefore expect that fast-switching SiC-based converters with dead-time of 1 µs or less, would significantly increase the performance. However, this cannot be verified experimentally in the laboratory at this time. Experimental

VI. Conclusion

The cascaded model predictive control (CMPC) algorithm for grid-connected converters with LCL filter has been improved and implemented in low-cost hardware utilizing both programmable logic and microprocessors available in the Xilinx ZynQ system-on-chip (SoC) device.

Simulations showed the method to be unsuitable for IGBT-based converters, due to high switching frequency and performance issues with large dead-time. These simulations were verified by experimental results. While dead-time compensation could reduce the harmonic distortion, high switching frequency gives unacceptable low efficiency.

The CMPC algorithm in its current implementation appears well suited for fast switching wide-bandgap transistors, such as silicon carbide (SiC). Simulations suggest an average switching frequency within normal operating limits for SiC, while short dead-time suggests low harmonic distortion. Comparison to conventional voltage oriented control (VOC) is not included in this paper, but results in [20] indicates that the cascaded MPC algorithm has reduced transient time after a step change in reference current.

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